

# 600 nA, Non-Unity Gain Rail-to-Rail Input/Output Op Amps

### Features

- Low Quiescent Current: 600 nA/Amplifier (typ.)
- Stable for gains of 10 V/V or higher
- Rail-to-Rail Input: -0.3V (min.) to V<sub>DD</sub> + 0.3V (max.)
- Rail-to-Rail Output:
- V<sub>SS</sub>+10 mV (min.) to V<sub>DD</sub>-10 mV (max.)
- Gain Bandwidth Product: 100 kHz (typ.)
- Wide Supply Voltage Range: 1.4V to 5.5V (max.)
- · Available in Single, Dual and Quad
- Chip Select (CS) with MCP6143

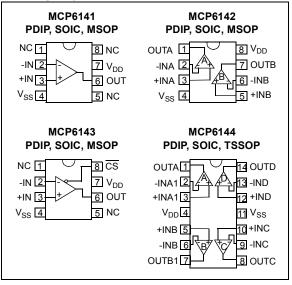
# Applications

- Toll Booth Tags
- Wearable Products
- Temperature Measurement
- Battery-Powered

## **Available Tools**

- · Spice macro models (at www.microchip.com)
- FilterLab<sup>®</sup> Software (at <u>www.microchip.com</u>)

### Package Types



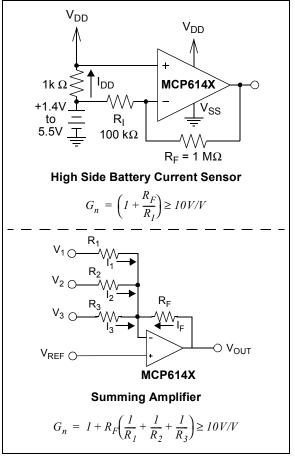
### Description

The MCP6141/2/3/4 family of non-unity gain stable operational amplifiers (op amps) from Microchip Technology, Inc. operate with a single supply voltage as low as 1.4V, while drawing less than 1  $\mu$ A (max.) of quiescent current per amplifier. These devices are also designed to support rail-to-rail input and output swing.

The MCP6141/2/3/4 op amps have a gain bandwidth product of 100 kHz (typ.) and are stable for gains of 10 V/V or higher. This specification makes these devices appropriate for battery-powered applications where higher frequency responses from the amplifier are required.

The MCP6141/2/3/4 family of op amps are offered in single (MCP6141), single with a Chip Select (CS) feature (MCP6143), dual (MCP6142) and quad (MCP6144) configurations.

# **Typical Applications**



# 1.0 ELECTRICAL CHARACTERISTICS

# 1.1 Maximum Ratings†

V <sub>DD</sub> - V <sub>SS</sub>	7.0V
All inputs and outputs	$V_{\rm SS}$ -0.3V to $V_{\rm DD}$ +0.3V
Difference Input voltage	V <sub>DD</sub> - V <sub>SS</sub>
Output Short Circuit Current	continuous
Current at Input Pins	±2 mA
Current at Output and Supply Pins	±30 mA
Storage temperature	65°C to +150°C
Junction Temperature, T <sub>J</sub>	+150°C
ESD protection on all pins (HBM:MM).	≥4 kV:200 V

**†Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

# PIN FUNCTION TABLE

Name	Function
+IN/+INA/+INB/+INC/+IND	Non-inverting Inputs
-IN/-INA/-INB/-INC/-IND	Inverting Inputs
V <sub>DD</sub>	Positive Power Supply
V <sub>SS</sub>	Negative Power Supply
OUT/OUTA/OUTB/OUTC/OUTD	Outputs
CS	Chip Select
NC	No internal connection

DC ELECTRICAL	<b>SPECIFICATIONS</b>
---------------	-----------------------

Electrical Characteristics: Unless otherwise indicated, all limits are specified for V <sub>DD</sub> = +1.4V to +5.5V, V <sub>SS</sub> = GND, T <sub>A</sub> = 25°C,								
$V_{CM} = V_{DD}/2$ , $R_L = 1 M\Omega$ to $V_{DD}/2$ , and $V_{OUT} \sim V_{DD}/2$ .								
_	-		_					

Parameters	Sym	Min	Тур	Max	Units	Conditions
Input Offset						V <sub>CM</sub> = V <sub>SS</sub>
Input Offset Voltage	V <sub>OS</sub>	-3.0	_	+3.0	mV	
Drift with Temperature	$\Delta V_{OS} / \Delta T$	_	±1.5	_	μV/°C	$T_A$ = -40°C to +85°C
Power Supply Rejection	PSRR	70	85	_	dB	
Input Bias Current and Impedance						
Input Bias Current	I <sub>B</sub>	_	1.0	_	pА	
Input Bias Current Over-Temperature	Ι <sub>Β</sub>	_	_	100	pА	$T_A$ = -40°C to +85°C
Input Offset Current	I <sub>OS</sub>	_	1.0	_	pА	
Common Mode Input Impedance	Z <sub>CM</sub>	_	10 <sup>13</sup>   6	_	Ω  pF	
Differential Input Impedance	Z <sub>DIFF</sub>	_	10 <sup>13</sup>   6	_	Ω  pF	
Common Mode	•					
Common-Mode Input Range	VCMR	V <sub>SS</sub> - 0.3	_	V <sub>DD</sub> + 0.3	V	
Common-Mode Rejection Ratio	CMRR	62	80	_	dB	V <sub>DD</sub> = 5V, V <sub>CM</sub> = -0.3V to 5.3V
		60	75	_	dB	V <sub>DD</sub> = 5V, V <sub>CM</sub> = 2.5V to 5.3V
		60	80	_	dB	V <sub>DD</sub> = 5V, V <sub>CM</sub> = -0.3V to 2.5V
Open Loop Gain						
DC Open Loop Gain (large signal)	A <sub>OL</sub>	95	115	_	dB	$R_L$ = 50 kΩ to V <sub>DD</sub> /2, 100 mV < V <sub>OUT</sub> < (V <sub>DD</sub> - 100 mV)
Output						
Maximum Output Voltage Swing	V <sub>OL</sub> , V <sub>OH</sub>	V <sub>SS</sub> + 10	_	V <sub>DD</sub> - 10	mV	$R_L$ = 50 k $\Omega$ to $V_{DD}/2$
Output Short Circuit Current	Ι <sub>Ο</sub>	_	21	_	mA	V <sub>OUT</sub> = 2.5V, V <sub>DD</sub> = 5 V
Power Supply						
Supply Voltage	V <sub>DD</sub>	1.4	_	5.5	V	
Quiescent Current per amplifier	I <sub>O</sub>	0.3	0.6	1.0	μA	I <sub>O</sub> = 0

# AC ELECTRICAL SPECIFICATIONS

	<b>Electrical Characteristics:</b> Unless otherwise indicated, all limits are specified for $V_{DD}$ = +5V, $V_{SS}$ = GND, $T_A$ = 25 °C,								
	$V_{CM} = V_{DD}/2$ , $R_L = 1 M\Omega$ to $V_{DD}/2$ , $C_L = 60 \text{ pF}$ , and $V_{OUT} \sim V_{DD}/2$ .								
Parameters Sym Min Typ Max Units Condit						Conditions			

Gain Bandwidth Product	GBWP	_	100	—	kHz	
Slew Rate	SR	_	24	—	V/ms	
Phase Margin	PM	_	60	—	0	G = +10
Input Voltage Noise	En		5.0	—	μVp-р	f = 0.1 Hz to 10 Hz
Input Voltage Noise Density	e <sub>n</sub>	_	170	—	nV/√Hz	f = 1 kHz
Input Current Noise Density	i <sub>n</sub>	_	0.6	—	fA/√Hz	f = 1 kHz

# SPECIFICATIONS FOR MCP6143 CHIP SELECT FEATURE

<b>Electrical Characteristics:</b> Unless otherwise indicated, all limits are specified for $V_{DD}$ = +1.4V to +5.5V, $V_{SS}$ = GND, $T_A$ = 25 °C, $V_{CM}$ = $V_{DD}/2$ , $R_L$ = 1 M $\Omega$ to $V_{DD}/2$ , $C_L$ = 60 pF, and $V_{OUT} \sim V_{DD}/2$ .								
Parameters	Sym	Min	Тур	Max	Units	Conditions		
CS Low Specifications								
CS Logic Threshold, Low	V <sub>IL</sub>	V <sub>SS</sub>	_	V <sub>SS</sub> + 0.3	V	For entire V <sub>DD</sub> range		
CS Input Current, Low	I <sub>CSL</sub>	_	5.0	_	pА	$\overline{\text{CS}} = \text{V}_{\text{SS}}$		
CS High Specifications								
CS Logic Threshold, High	V <sub>IH</sub>	V <sub>DD</sub> - 0.3		V <sub>DD</sub>	V	For entire V <sub>DD</sub> range		
CS Input Current, High	I <sub>CSH</sub>	_	5.0	_	pА	$\overline{\text{CS}} = \text{V}_{\text{DD}}$		
CS Input High, GND Current	Ι <sub>Q</sub>	_	20	_	pА	$\overline{\text{CS}} = \text{V}_{\text{DD}}$		
Amplifier Output Leakage, $\overline{\text{CS}}$ High		_	20	_	pА	$\overline{\text{CS}} = \text{V}_{\text{DD}}$		
Dynamic Specifications								
CS Low to Amplifier Output High Turn-on Time	t <sub>ON</sub>	_	2.0	50	ms	$\overline{\text{CS}} \text{ low} = \text{V}_{\text{SS}} + 0.3 \text{V}, \text{ G} = +1 \text{ V/V}, \\ \text{V}_{\text{OUT}} = 0.9 \text{ V}_{\text{DD}}/2$		
$\overline{\text{CS}}$ High to Amplifier Output High Z	t <sub>OFF</sub>	_	10	_	μs	$\overline{\text{CS}} \text{ high = V}_{\text{DD}} - 0.3 \text{V}, \text{ G} = +1 \text{ V/V}$ $\text{V}_{\text{OUT}} = 0.1 \text{ V}_{\text{DD}}/2$		
Hysteresis	V <sub>HYST</sub>	_	0.6	_	V	V <sub>DD</sub> = 5V		

# **TEMPERATURE SPECIFICATIONS**

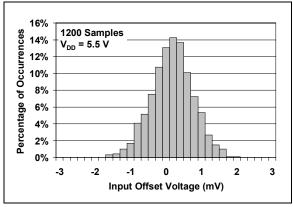
Electrical Characteristics: Unless otherwise indicated, all limits are specified for V <sub>DD</sub> = +1.4V to +5.5V, V <sub>SS</sub> = GND.									
Parameters	Symbol	Min	Тур	Max	Units	Conditions			
Temperature Ranges									
Specified Temperature Range	T <sub>A</sub>	-40	_	+85	°C				
Operating Temperature Range	T <sub>A</sub>	-40	_	+125	°C	Note 1			
Storage Temperature Range	T <sub>A</sub>	-65	_	+150	°C				
Thermal Package Resistances									
Thermal Resistance, 8L-PDIP	$\theta_{JA}$	—	85	—	°C/W				
Thermal Resistance, 8L-SOIC	$\theta_{JA}$	_	163	_	°C/W				
Thermal Resistance, 8L-MSOP	$\theta_{JA}$	—	206	—	°C/W				
Thermal Resistance, 14L-PDIP	$\theta_{JA}$	_	70	_	°C/W				
Thermal Resistance, 14L-SOIC	$\theta_{JA}$	_	108	_	°C/W				
Thermal Resistance, 14L-TSSOP	$\theta_{JA}$	_	100	_	°C/W				

Note 1: The MCP6141/2/3/4 family of op amps operates over this extended range, but with reduced performance.

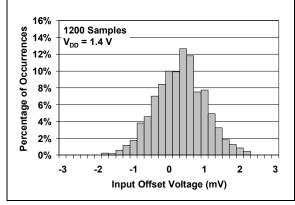
# 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

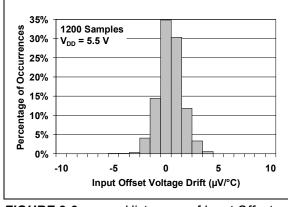
**Note:** Unless otherwise indicated,  $V_{DD}$  = +5V,  $V_{SS}$  = GND,  $T_A$  = 25°C,  $V_{CM}$  =  $V_{DD}/2$ ,  $R_L$  = 1 M $\Omega$  to  $V_{DD}/2$ ,  $C_L$  = 60 pF, and  $V_{OUT} \sim V_{DD}/2$ .



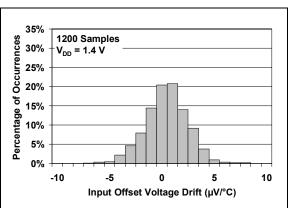
**FIGURE 2-1:** Histogram of Input Offset Voltage with  $V_{DD} = 5.5V$ .



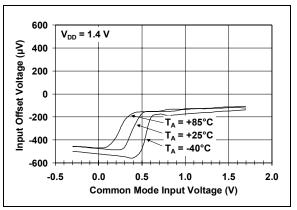
**FIGURE 2-2:** Histogram of Input Offset Voltage with  $V_{DD} = 1.4V$ .



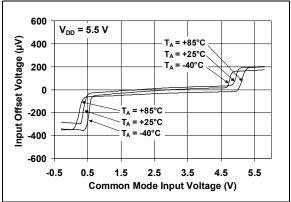
**FIGURE 2-3:** Histogram of Input Offset Voltage Drift with  $V_{DD} = 5.5V$ .



**FIGURE 2-4:** Histogram of Input Offset Voltage Drift with  $V_{DD} = 1.4V$ .



**FIGURE 2-5:** Input Offset Voltage vs. Common Mode Input Voltage vs. Temperature with  $V_{DD} = 1.4V$ .



**FIGURE 2-6:** Input Offset Voltage vs. Common Mode Input Voltage vs. Temperature with  $V_{DD} = 5.5V$ .

**Note:** Unless otherwise indicated,  $V_{DD}$  = +5V,  $V_{SS}$  = GND,  $T_A$  = 25°C,  $V_{CM}$  =  $V_{DD}/2$ ,  $R_L$  = 1 M $\Omega$  to  $V_{DD}/2$ ,  $C_L$  = 60 pF, and  $V_{OUT} \sim V_{DD}/2$ .

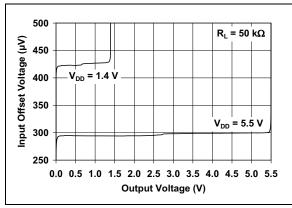


FIGURE 2-7:Input Offset Voltage vs.Output Voltage vs. Power Supply Voltage.

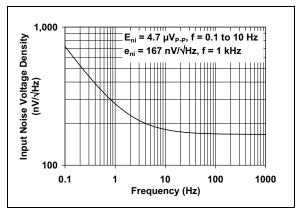
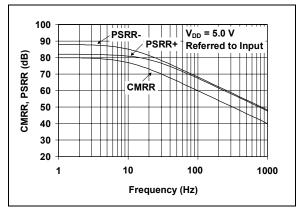
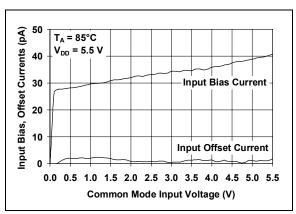


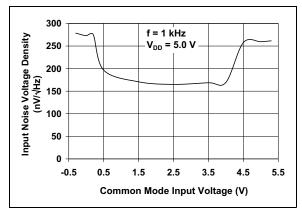
FIGURE 2-8: Input Noise Voltage Density vs. Frequency.



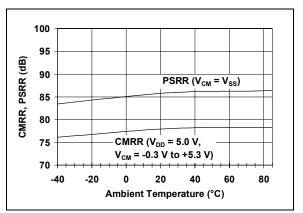
**FIGURE 2-9:** Common Mode Rejection Ratio, Power Supply Rejection Ratio vs. Frequency.



**FIGURE 2-10:** Input Bias, Offset Currents vs. Common Mode Input Voltage with Temperature = 85°C.

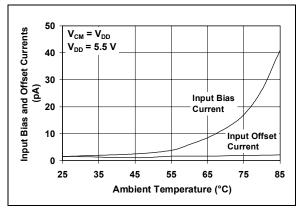


**FIGURE 2-11:** Input Noise Voltage Density vs. Common Mode Input Voltage.

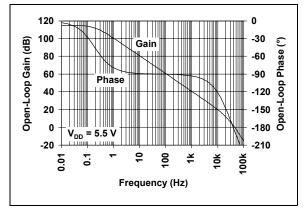


**FIGURE 2-12:** Common Mode Rejection Ratio, Power Supply Rejection Ratio vs. Ambient Temperature.

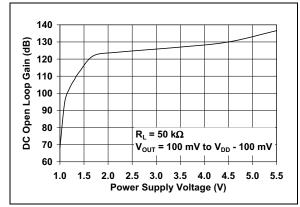
**Note:** Unless otherwise indicated,  $V_{DD}$  = +5V,  $V_{SS}$  = GND,  $T_A$  = 25°C,  $V_{CM}$  =  $V_{DD}/2$ ,  $R_L$  = 1 M $\Omega$  to  $V_{DD}/2$ ,  $C_L$  = 60 pF, and  $V_{OUT} \sim V_{DD}/2$ .



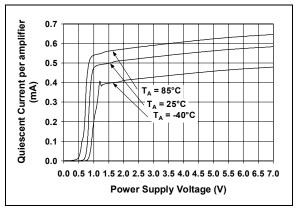




**FIGURE 2-14:** Open Loop Gain, Phase vs. Frequency with  $V_{DD} = 5.5V$ .



**FIGURE 2-15:** DC Open Loop Gain vs. Power Supply Voltage.



**FIGURE 2-16:** Quiescent Current Vs. Power Supply Voltage vs. Temperature.

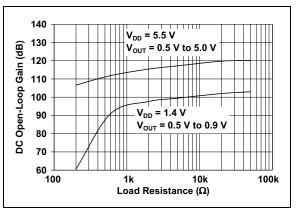
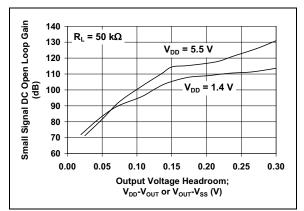
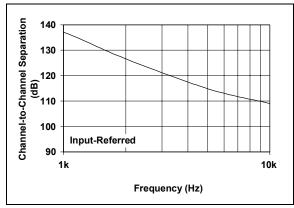


FIGURE 2-17: DC Open Loop Gain vs. Load Resistance vs. Power Supply Voltage.

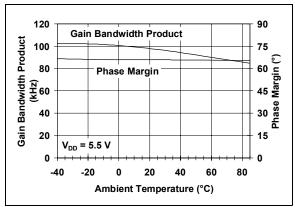


**FIGURE 2-18:** Small Signal DC Open Loop Gain vs. Output Voltage Headroom vs. Power Supply.

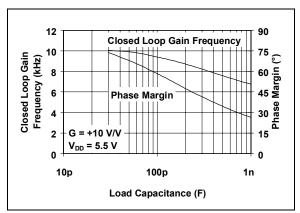
**Note:** Unless otherwise indicated,  $V_{DD}$  = +5V,  $V_{SS}$  = GND,  $T_A$  = 25°C,  $V_{CM}$  =  $V_{DD}/2$ ,  $R_L$  = 1 M $\Omega$  to  $V_{DD}/2$ ,  $C_L$  = 60 pF, and  $V_{OUT} \sim V_{DD}/2$ .



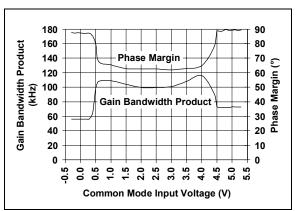
**FIGURE 2-19:** Channel to Channel Separation vs. Frequency (MCP6142 and MCP6144 only).



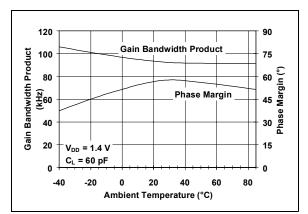
**FIGURE 2-20:** Gain Bandwidth Product, Phase Margin vs. Ambient Temperature with  $V_{DD} = 5.5V$ .



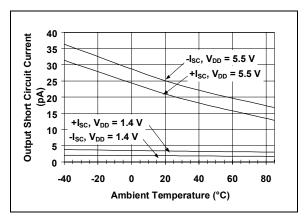
**FIGURE 2-21:** Closed Loop Gain Frequency, Phase Margin vs. Load Capacitance with  $V_{DD} = 5.5V$ .



**FIGURE 2-22:** Gain Bandwidth Product, Phase Margin vs. Common Mode Input Voltage.

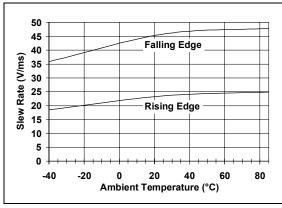


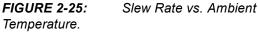
**FIGURE 2-23:** Gain Bandwidth Product, Phase Margin vs. Ambient Temperature with  $V_{DD} = 1.4V$ .

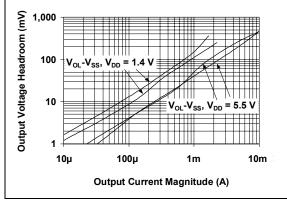


**FIGURE 2-24:** Output Short Circuit Current vs. Ambient Temperature vs. Power Supply Voltage.

**Note:** Unless otherwise indicated,  $V_{DD}$  = +5V,  $V_{SS}$  = GND,  $T_A$  = 25°C,  $V_{CM}$  =  $V_{DD}/2$ ,  $R_L$  = 1 M $\Omega$  to  $V_{DD}/2$ ,  $C_L$  = 60 pF, and  $V_{OUT} \sim V_{DD}/2$ .







**FIGURE 2-26:** Output Voltage Headroom vs. Output Current Magnitude vs. Power Supply Voltage.

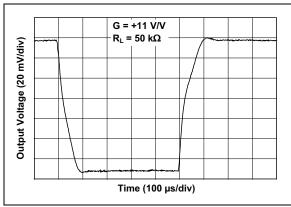
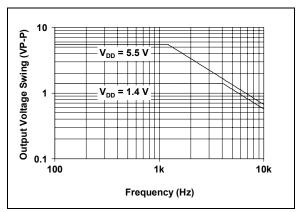
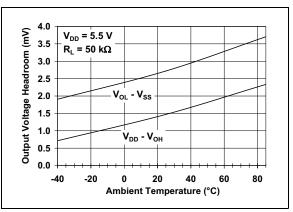


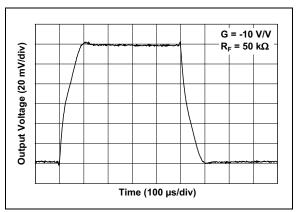
FIGURE 2-27: Small Signal Non-Inverting Pulse Response vs. Time.



**FIGURE 2-28:** Output Voltage Swing vs. Frequency vs. Power Supply Voltage.



**FIGURE 2-29:** Output Voltage Headroom vs. Ambient Temperature with  $V_{DD} = 5.5V$ .



**FIGURE 2-30:** Small Signal Inverting Pulse Response vs. Time.

**Note:** Unless otherwise indicated,  $V_{DD}$  = +5V,  $V_{SS}$  = GND,  $T_A$  = 25°C,  $V_{CM}$  =  $V_{DD}/2$ ,  $R_L$  = 1 M $\Omega$  to  $V_{DD}/2$ ,  $C_L$  = 60 pF, and  $V_{OUT} \sim V_{DD}/2$ .

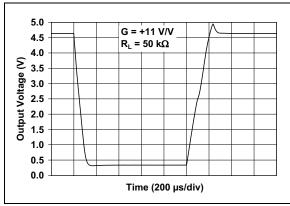
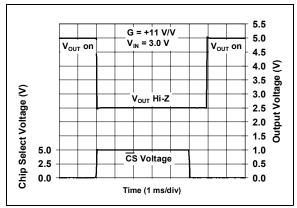
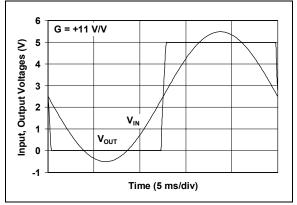


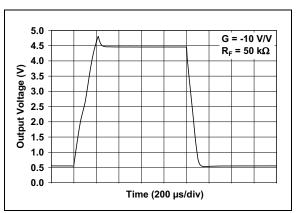
FIGURE 2-31: Large Signal Non-Inverting Pulse Response vs. Time.



**FIGURE 2-32:** Chip Select ( $\overline{CS}$ ) to Amplifier Output Response Time (MCP6143 only).



**FIGURE 2-33:** The MCP6141/2/3/4 family shows no phase reversal (for information only–the Maximum Absolute Input Voltage is still  $V_{SS}$  - 0.3V and  $V_{DD}$  + 0.3V).



**FIGURE 2-34:** Large Signal Inverting Pulse Response vs. Time.

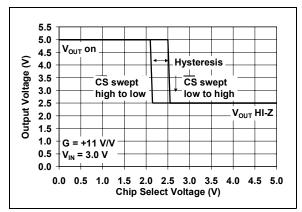


FIGURE 2-35: Output Voltage vs. Chip Select (CS) Voltage (MCP6143 only).

# 3.0 APPLICATIONS INFORMATION

The MCP6141/2/3/4 family of operational amplifiers are fabricated on Microchip's state-of-the-art CMOS process. They are stable for noise gain of 10 V/V or higher. Microchip also produces a unity gain stable product, the MCP6041/2/3/4 family, which has similar specifications. The MCP6041/2/3/4 family has a bandwidth of 1.4 kHz at a noise gain of 10 V/V, while the MCP6141/2/3/4 family has a bandwidth of 10 kHz at a noise gain of 10 V/V. These devices are suitable for a wide range of applications requiring very low power consumption. With these op amps, the power supply pin needs to be bypassed with a 0.1  $\mu$ F capacitor.

### 3.1 Rail-to-Rail Input

The input stage of these devices uses two differential input stages in parallel; one operates at low V<sub>CM</sub> (common mode input voltage) and the other at high V<sub>CM</sub>. With this topology, the MCP6141/2/3/4 family operates with V<sub>CM</sub> up to 300 mV past either supply rail. The Input Offset Voltage is measured at both V<sub>CM</sub> = V<sub>SS</sub> - 0.3V and V<sub>DD</sub> + 0.3V to ensure proper operation.

# 3.2 Output Loads and Battery Life

The MCP6141/2/3/4 op amp family has low quiescent current, which supports battery-powered applications. There is minimal quiescent current glitch when chip select ( $\overline{CS}$ ) is raised or lowered. This prevents excessive current draw and reduced battery life when the part is turned off or on.

Heavy resistive loads at the output can cause excessive battery drain. Driving a DC voltage of 2.5V across a 100 k $\Omega$  load resistor will cause the supply current to increase by 25  $\mu A$ , depleting the battery 43 times as fast as I\_{\Omega} (0.6  $\mu A$  typ) alone.

High frequency signals (fast edge rate) across capacitive loads will also significantly increase supply current. For instance, a 0.1  $\mu F$  capacitor at the output presents an AC impedance of 15.9 k $\Omega$  (1/2 $\pi fC$ ) to a 100 Hz sinewave. It can be shown that the average power drawn from the battery by a 5.0 V<sub>p-p</sub> sinewave (1.77 Vrms) under these conditions is:

#### EQUATION

$$\begin{split} P_{SUPPLY} &= (V_{DD} - V_{SS})(I_Q + V_{L(p-p)}fC_L) \\ &= (5V)(0.6\mu A + 5.0V_{p-p} \cdot 100Hz \cdot 0.1\mu F) \\ &= 3.0\mu W + 50\mu W \end{split}$$

This will drain the battery 18 times as fast as  $I_{Q}$  alone.

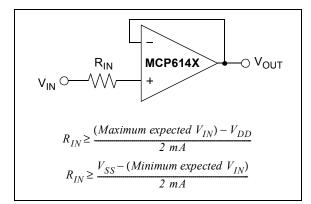
### 3.3 Rail-to-Rail Output

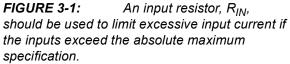
The MCP6141/2/3/4 family Maximum Output Voltage Swing defines the maximum swing possible under a particular output load. According to the specification table, the output can reach up to 10 mV of either supply rail with a 50 k $\Omega$  load.

### 3.4 Input Voltage and Phase Reversal

The MCP6141/2/3/4 op amp family uses CMOS transistors at the input. It is designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-33 shows an input voltage exceeding both supplies without output phase reversal.

The maximum operating V<sub>CM</sub> that can be applied to the inputs is V<sub>SS</sub> -0.3V and V<sub>DD</sub> + 0.3V. Voltage on the input that exceeds this absolute maximum rating can cause excessive current to flow in or out of the input pins. Current beyond ±2 mA can cause possible reliability problems. Applications that exceed this rating must be externally limited with an input resistor, as shown in Figure 3-1.

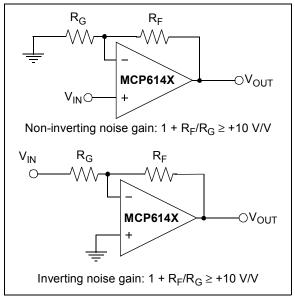




# 3.5 Stability

The MCP6141/2/3/4 op amp family is designed to give high bandwidth and faster slew rate for circuits with high noise ( $G_n$ ) or signal gain. The related unity-gain stable MCP6041/2/3/4 op amp family has lower AC performance, but it is preferable for low noise gain applications.

Noise gain is defined to be the gain from a voltage source at the non-inverting input to the output when all other voltage sources are zeroed (shorted out). Noise gain is independent of signal gain and depends only on components in the feedback loop.



**FIGURE 3-2:** Noise gain for inverting and non-inverting amplifier configuration.

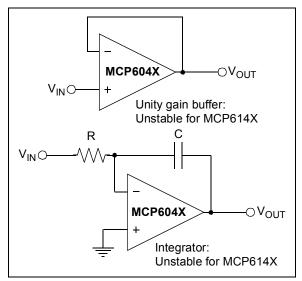
Figure 3-2 shows non-inverting and inverting amplifier circuits. In order for the amplifiers to be stable, the noise gain should meet the specified requirement:

#### EQUATION

$$G_n = 1 + \frac{R_F}{R_G} \ge 10V/V$$

Note that an inverting signal gain of G = -9 V/V corresponds to a noise gain  $G_n$  = +10 V/V.

Figure 3-3 shows a unity gain buffer and integrator that are unstable when used with the MCP6141/2/3/4 family. However, they are suitable for the MCP6041/2/3/4 family.



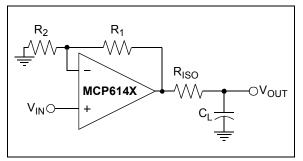
**FIGURE 3-3:** Typical Circuits that are not suitable for the MCP6141/2/3/4 family.

Note that the integrator circuit in Figure 3-3 becomes unity gain at high frequencies because of the capacitor. Therefore, this circuit is unstable for the MCP6141/2/3/4.

# 3.6 Capacitive Load and Stability

Driving capacitive loads can cause stability problems with voltage feedback op amps. Figure 2-21 shows how increasing the load capacitance will decrease the phase margin. While a phase margin above 60° is ideal, 45° is on the verge of instability. As can be seen, up to  $C_L = 150 \text{ pF}$  can be placed on the MCP6141/2/3/4 op amp outputs without any problems, while 250 pF creates a 45° phase margin.

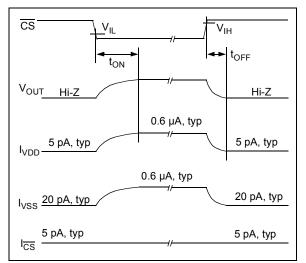
When the op amp is required to drive large capacitive loads ( $C_L > 150 \text{ pF}$ ), a small series resistor ( $R_{ISO}$  in Figure 3-4) at the output of the amplifier improves the phase margin. This resistor makes the output load resistive at higher frequencies, which improves the phase margin. The bandwidth reduction caused by the capacitive load, however, is not changed. To select  $R_{ISO}$ , start with 1 k $\Omega$ , then use the MCP6141 SPICE macro model and bench testing to adjust  $R_{ISO}$  until there is a minimum frequency response peaking.



*FIGURE 3-4:* Amplifier circuit for heavy capacitive loads.

## 3.7 The MCP6143 Chip Select (CS) Option

The MCP6143 is a single amplifier with a chip select (CS) option. When CS is pulled high, the supply current drops to 20 pA (typ.) and goes through the CS pin to  $V_{SS}$ . When this happens, the amplifier is put into a high impedance state. By pulling CS low, the amplifier is enabled. If the CS pin is left floating, the amplifier will not operate properly. Figure 3-5 shows the output voltage and supply current response to a CS pulse.



**FIGURE 3-5:** Timing Diagram for the  $\overline{CS}$  function on the MCP6143 op amp.

# 3.8 Layout Considerations

Good PC board layout techniques will help you achieve the performance shown in the specifications and typical performance curves. It will also assist in minimizing Electro-Magnetic Compatibility (EMC) issues.

### 3.8.1 SURFACE LEAKAGE

In applications where low input bias current is critical, PC board surface leakage effects and signal coupling from trace to trace need to be considered.

Surface leakage is caused by a difference in voltage between traces, combined with high humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is  $10^{12}\Omega$ . A 5V difference would cause 5 pA of current to flow, which is greater than the input current of the MCP6141/2/3/4 family at 25°C (1 pA, typ).

The simplest technique to reduce surface leakage is using a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin or trace. Figure 3-6 shows an example of a typical layout.

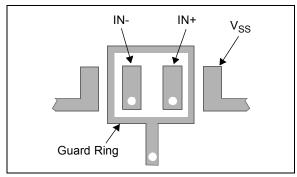
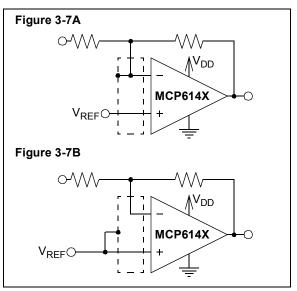


FIGURE 3-6: Example of Guard Ring layout.

Circuit schematics for different guard ring implementations are shown in Figure 3-7. Figure 3-7A biases the guard ring to the input common mode voltage, which is most effective for non-inverting gains. Figure 3-7B biases the guard ring to a reference voltage ( $V_{REF}$ , which can be ground), which is useful for inverting gains and precision photo sensing circuits.



**FIGURE 3-7:** Two possible guard ring connection strategies to reduce surface leakage effects.

#### 3.8.2 COMPONENT PLACEMENT

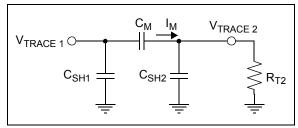
In order to help prevent crosstalk:

- Separate digital components from analog components, and low speed devices from high speed devices.
- Keep sensitive traces short and straight. Separate them from interfering components and traces. This is especially important for high frequency (low rise time) signals.
- Use a 0.1  $\mu F$  supply bypass capacitor within 0.1" (2.5 mm) of the  $V_{DD}$  pin. It must connect directly to the ground plane.

### 3.8.3 SIGNAL COUPLING

The input pins of the MCP6141/2/3/4 family of op amps are high impedance, which allows noise injection. This noise can be capacitively or magnetically coupled. In either case, using a ground plane helps reduce noise injection.

When noise is coupled capacitively, the ground plane provides shunt capacitance to ground for high frequency signals (Figure 3-8 shows the equivalent circuit). The coupled current,  $I_M$ , produces a lower voltage ( $V_{TRACE 2}$ ) on the victim trace when the trace to ground plane capacitance ( $C_{SH2}$ ) is large and the terminating resistor ( $R_{T2}$ ) is small. Increasing the distance between traces and using wider traces also helps.



**FIGURE 3-8:** Equivalent circuit for capacitive coupling between traces on a PC board (with ground plane).

When noise is coupled magnetically, the ground plane reduces the mutual inductance between traces. This occurs because the ground return current at high frequencies will follow a path directly beneath the signal trace. Increasing the separation between traces makes a significant difference. Changing the direction of one of the traces can also reduce magnetic coupling.

If these techniques are not enough, it may help to place guard traces next to the victim trace. They should be on both sides of the victim trace and be as close as possible. Connect the guard traces to ground plane at both ends and in the middle for long traces.

#### 3.9 Typical Applications

#### 3.9.1 BATTERY CURRENT SENSING

The MCP6141/2/3/4 op amps' Common Mode Input Range, which goes 300 mV beyond both supply rails, supports their use in high side and low side battery current sensing applications. The very low quiescent current (0.6  $\mu$ A, typ.) help prolong battery life, while the rail-to-rail output allows you to detect low currents.

Figure 3-9 shows a high side battery current sensor circuit. The feedback and input resistors are sized to minimize power losses. The battery current (I<sub>DD</sub>) through the 1 k $\Omega$  resistor causes its top terminal to be more negative than the bottom terminal. This keeps the common mode input voltage of the op amp  $\leq$  V<sub>DD</sub>, which is within its allowed range. The output of the op amp can reach V<sub>DD</sub> - 0.1 mV (see Figure 2-26), which is a smaller error than the offset voltage.

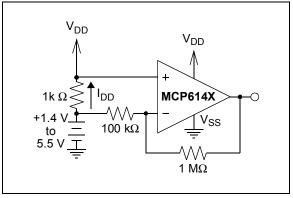


FIGURE 3-9: High Side Battery Current Sensor.

#### 3.9.2 SUMMING AMPLIFIER

The rail-to-rail input and output, the 600 nA (typ.) quiescent current and the wide bandwidth make the MCP6141/2/3/4 family of operational amplifiers fit well in a summing amplifier circuit, as shown in Figure 3-10.

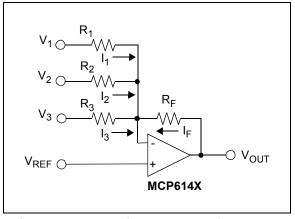


FIGURE 3-10: Summing amplifier circuit.

In this configuration, the amplifier outputs the sum of the three input voltages. The ratio of the sum and the output voltage is defined using the feedback and input resistors.  $V_{REF}$  is used to offset the output voltage. This family of amplifiers is stable for noise gain (G<sub>n</sub>) of 10 V/V or higher. The G<sub>n</sub> and the signal gain of the summing amplifier is calculated as shown below:

#### EQUATION

Noise Gain:
$G_n = 1 + R_F \left( \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right) \ge 10 \ V/V$
Signal Gain:
$V_{0I} = \frac{-R_F}{R_I} \times V_I$
$V_{02} = \frac{-R_F}{R_2} \times V_2$
$V_{03} = \frac{-R_F}{R_3} \times V_3$
$V_{04} = \left(I + \frac{R_F}{R_I} + \frac{R_F}{R_2} + \frac{R_F}{R_3}\right) \times V_{REF}$
$V_{OUT} = V_{01} + V_{02} + V_{03} + V_{04}$
$V_{OUT} = R_F \left[ \frac{V_{REF} - V_I}{R_I} + \frac{V_{REF} - V_2}{R_2} + \frac{V_{REF} - V_3}{R_3} \right] + V_{REF}$

At a noise gain of 10 V/V, the amplifier bandwidth is approximately 10 kHz. The bandwidth to quiescent current ratio of MCP6141/2/3/4 makes this device an appropriate choice for battery-powered applications.

# 4.0 SPICE MACRO MODEL

The Spice macro model for the MCP6141, MCP6142, MCP6143 and MCP6144 simulates the typical amplifier performance of offset voltage, DC power supply rejection, input capacitance, DC common mode rejection, open loop gain over frequency, phase margin, output swing, DC power supply current, power supply current change with supply voltage, input common mode range, output voltage range vs. load and input voltage noise.

The characteristics of the MCP6141, MCP6142, MCP6143 and MCP6144 amplifiers are similar in terms of performance and behavior. This single op amp macro model supports all four devices, with the exception of the chip select function of the MCP6143, which is not modeled.

The listing for this macro model is shown on the next page. The most recent revision of the model can be downloaded from Microchip's web site at <u>www.microchip.com</u>.

#### Software License Agreement

The software supplied herewith by Microchip Technology Incorporated (the "Company") is intended and supplied to you, the Company's customer, for use solely and exclusively on Microchip products.

The software is owned by the Company and/or its supplier, and is protected under applicable copyright laws. All rights are reserved. Any use in violation of the foregoing restrictions may subject the user to criminal sanctions under applicable laws, as well as to civil liability for the breach of the terms and conditions of this license.

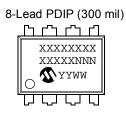
THIS SOFTWARE IS PROVIDED IN AN "AS IS" CONDITION. NO WARRANTIES, WHETHER EXPRESS, IMPLIED OR STATU-TORY, INCLUDING, BUT NOT LIMITED TO, IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICU-LAR PURPOSE APPLY TO THIS SOFTWARE. THE COMPANY SHALL NOT, IN ANY CIRCUMSTANCES, BE LIABLE FOR SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES, FOR ANY REASON WHATSOEVER.

```
.SUBCKT MCP6141 1 2 3 4 5
                | | Output
                  | | Negative Supply
                 | Positive Supply
                | Inverting Input
               Non-inverting Input
* Macromodel for the MCP6141/2/3/4 op amp family:
   MCP6141 (single)
   MCP6142 (dual)
   MCP6143 (single w/ CS; chip select is not modeled)
   MCP6144 (quad)
* Revision History:
   REV A: 06-Sep-02, KEB (created model)
* Recommendations:
   Use PSPICE (or SPICE 2G6; other simulators may require translation)
   For a quick, effective design, use a combination of: data sheet
     specs, bench testing, and simulations with this macromodel
   For high impedance circuits, set GMIN=100F in the .OPTIONS
     statement
* Supported:
   Typical performance at room temperature (25 degrees C)
   DC, AC, Transient, and Noise analyses.
   Most specs, including: offsets, DC PSRR, DC CMRR, input impedance,
     open loop gain, voltage ranges, supply current, ..., etc.
* Not Supported:
   Chip select (MCP6143)
    Variation in specs vs. Power Supply Voltage
    Distortion (detailed non-linear behavior)
   Temperature analysis
   Process variation
   Behavior outside normal operating region
* Input Stage
V10 3 10 -300M
R10 10 11 258K
R11 10 12 258K
C11 11 12 3.53P
C12 1 0 6.00P
E12 1 14 POLY(4) 20 0 21 0 26 0 27 0 1.00M 117 117 1 1
I12 14 0 1.50P
M12 11 14 15 15 NMI L=2.00U W=5.00U
C13 14 2 6.00P
M14 12 2 15 15 NMI L=2.00U W=5.00U
I14 2 0 500E-15
C14 2 0 6.00P
```

I15 15 4 300N V16 16 4 200M D16 16 15 DL V13 3 13 50.0M D13 14 13 DL \* Noise, PSRR, and CMRR I20 21 20 423U D20 20 0 DN1 D21 0 21 DN1 G26 0 26 POLY(1) 3 4 308U -56.0U R26 26 0 1 G27 0 27 POLY(2) 1 3 2 4 -979U 178U 178U R27 27 0 1 \* Open Loop Gain, Slew Rate G30 0 30 POLY(1) 12 11 0 1.00K R30 30 0 1 E31 31 0 POLY(1) 3 4 29.3 1.05 D31 30 31 DL E32 0 32 POLY(1) 3 4 57.0 2.04 D32 32 30 DL G33 0 33 POLY(1) 30 0 0 562 R33 33 0 1 C33 33 0 838M G34 0 34 POLY(1) 33 0 0 1.00 R34 34 0 1.00 C34 34 0 8.53U G35 0 35 POLY(2) 34 0 33 34 0 1.00 1.22 R35 35 0 1.00 \* Output Stage G50 0 50 POLY(1) 57 5 0 1.00 D51 50 51 DL R51 51 0 1K D52 52 50 DL R52 52 0 1K G53 3 0 POLY(1) 51 0 300N 1M G54 0 4 POLY(1) 52 0 300N -1M E55 55 0 POLY(2) 3 0 51 0 -10M 1 -100M D55 57 55 DLS E56 56 0 POLY(2) 4 0 52 0 10M 1 -100M D56 56 57 DLS G57 0 57 POLY(3) 3 0 4 0 35 0 0 17.8U 17.8U 35.5U R57 57 0 28.2K R58 57 5 1.00 C58 5 0 2.00P \* Models .MODEL NMI NMOS .MODEL DL D N=1 IS=1F .MODEL DLS D N=10M IS=1F .MODEL DN1 D IS=1F KF=1.17E-18 AF=1 .ENDS MCP6141

# 5.0 PACKAGING INFORMATION

# 5.1 Package Marking Information

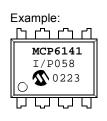


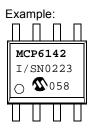
8-Lead SOIC (150 mil)



#### 8-Lead MSOP







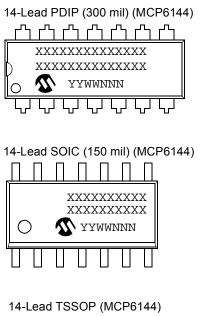
Example:

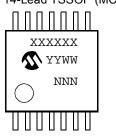


Legend	XXX YY WW NNN	Customer specific information* Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code					
	<b>Note</b> : In the event the full Microchip part number cannot be marked on one line, it wi be carried over to the next line thus limiting the number of available characters for customer specific information.						

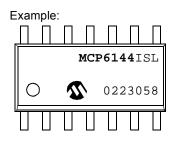
\* Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

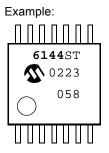
# 5.1 Package Marking Information (Continued)



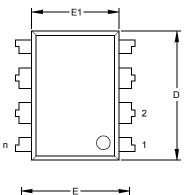


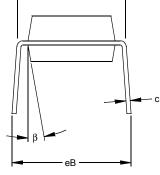
Example: MCP6144-I/P 0223058 UUUUUUUUU

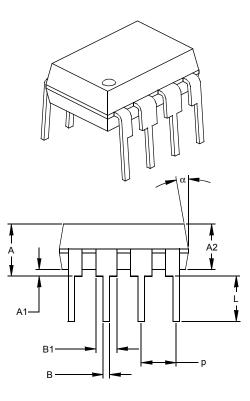




8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)







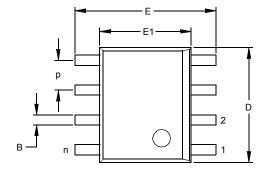
	Units		INCHES*		MILLIMETERS		
Dimensior	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	р		.100			2.54	
Top to Seating Plane	Α	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	В	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

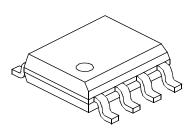
\* Controlling Parameter § Significant Characteristic

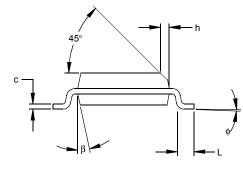
Notes: Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed

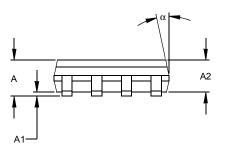
.010" (0.254mm) per side. JEDEC Equivalent: MS-001 Drawing No. C04-018

# 8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)









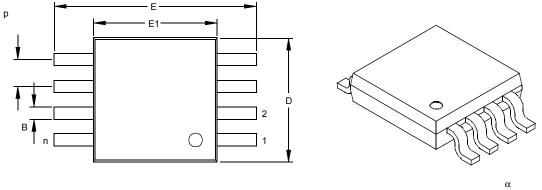
	Units		INCHES*		N	IILLIMETERS	5
Dimensi	on Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	р		.050			1.27	
Overall Height	А	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	С	.008	.009	.010	0.20	0.23	0.25
Lead Width	В	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

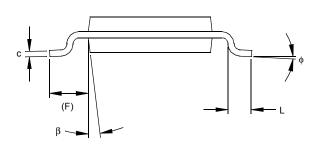
\* Controlling Parameter § Significant Characteristic

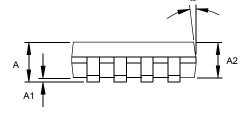
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-012 Drawing No. C04-057

# 8-Lead Plastic Micro Small Outline Package (MS) (MSOP)







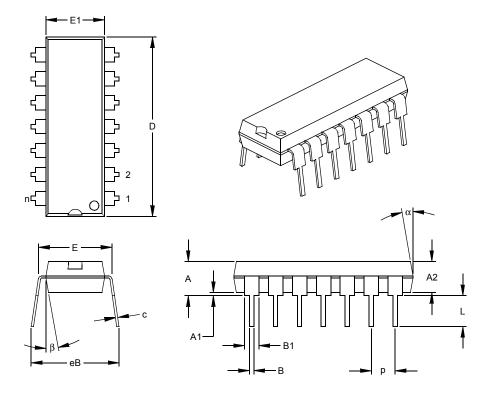
Units		INCHES		М	ILLIMETERS*	
on Limits	MIN	NOM	MAX	MIN	NOM	MAX
n		8				8
р	.026			0.65		
А			.044			1.18
A2	.030	.034	.038	0.76	0.86	0.97
A1	.002		.006	0.05		0.15
E	.184	.193	.200	4.67	4.90	.5.08
E1	.114	.118	.122	2.90	3.00	3.10
D	.114	.118	.122	2.90	3.00	3.10
L	.016	.022	.028	0.40	0.55	0.70
F	.035	.037	.039	0.90	0.95	1.00
¢	0		6	0		6
С	.004	.006	.008	0.10	0.15	0.20
В	.010	.012	.016	0.25	0.30	0.40
α		7			7	
β		7			7	
	n           n           p           A           A2           A1           E           E1           D           L           F           \$\phi\$           C           B           \$\alpha\$	on Limits         MIN           n         P           A         A           A2         .030           A1         .002           E         .184           E1         .114           D         .114           L         .016           F         .035           φ         0           C         .004           B         .010           α	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	$\begin{array}{c c c c c c c c c c c c c c c c c c c $

\*Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. Drawing No. C04-111

# 14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



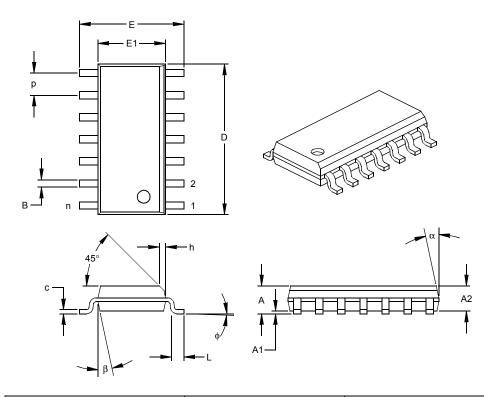
s MIN .140 .115	NOM 14 .100 .155	MAX	MIN	NOM 14	MAX
	.100			14	
	155			2.54	
115	.100	.170	3.56	3.94	4.32
.115	.130	.145	2.92	3.30	3.68
.015			0.38		
.300	.313	.325	7.62	7.94	8.26
.240	.250	.260	6.10	6.35	6.60
.740	.750	.760	18.80	19.05	19.30
.125	.130	.135	3.18	3.30	3.43
.008	.012	.015	0.20	0.29	0.38
.045	.058	.070	1.14	1.46	1.78
.014	.018	.022	0.36	0.46	0.56
.310	.370	.430	7.87	9.40	10.92
5	10	15	5	10	15
5	10	15	5	10	15
	.240 .740 .125 .008 .045 .014 .310	.240         .250           .740         .750           .125         .130           .008         .012           .045         .058           .014         .018           .310         .370           5         10	.240         .250         .260           .740         .750         .760           .125         .130         .135           .008         .012         .015           .045         .058         .070           .014         .018         .022           .310         .370         .430           5         10         15	.240         .250         .260         6.10           .740         .750         .760         18.80           .125         .130         .135         3.18           .008         .012         .015         0.20           .045         .058         .070         1.14           .014         .018         .022         0.36           .310         .370         .430         7.87           5         10         15         5	.240         .250         .260         6.10         6.35           .740         .750         .760         18.80         19.05           .125         .130         .135         3.18         3.30           .008         .012         .015         0.20         0.29           .045         .058         .070         1.14         1.46           .014         .018         .022         0.36         0.46           .310         .370         .430         7.87         9.40           5         10         15         5         10

\* Controlling Parameter § Significant Characteristic

Notes: Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed

.010" (0.254mm) per side. JEDEC Equivalent: MS-001 Drawing No. C04-005

14-Lead Plastic Small Outline (SL) - Narrow, 150 mil (SOIC)



	Units	INCHES*			MILLIMETERS		
Dimens	sion Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	р		.050			1.27	
Overall Height	Α	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	¢	0	4	8	0	4	8
Lead Thickness	С	.008	.009	.010	0.20	0.23	0.25
Lead Width	В	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15
* Controlling Parameter							

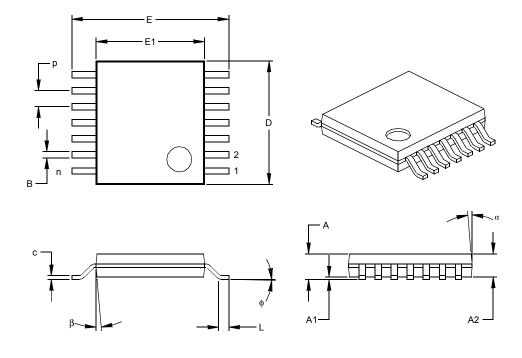
\* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimensio	n Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	р		.026			0.65	
Overall Height	А			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	Е	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	С	.004	.006	.008	0.09	0.15	0.20
Lead Width	B1	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

\* Controlling Parameter § Significant Characteristic

#### Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side. JEDEC Equivalent: MO-153 Drawing No. C04-087

NOTES:

# **ON-LINE SUPPORT**

Microchip provides on-line support on the Microchip World Wide Web site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape<sup>®</sup> or Microsoft<sup>®</sup> Internet Explorer. Files are also available for FTP download from our FTP site.

#### Connecting to the Microchip Internet Web Site

The Microchip web site is available at the following URL:

#### www.microchip.com

The file transfer site is available by using an FTP service to connect to:

#### ftp://ftp.microchip.com

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
- Technical Support Section with Frequently Asked
   Questions
- · Design Tips
- Device Errata
- Job Postings
- Microchip Consultant Program Member Listing
- Links to other useful web sites related to Microchip Products
- Conferences for products, Development Systems, technical information and more
- Listing of seminars and events

# SYSTEMS INFORMATION AND UPGRADE HOT LINE

The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive the most current upgrade kits. The Hot Line Numbers are:

1-800-755-2345 for U.S. and most of Canada, and

1-480-792-7302 for the rest of the world.

092002

# **READER RESPONSE**

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

To:	Technical Publications Manager	Total Pages Sent
RE:	Reader Response	
From	: Name	
	Company	
	Address	
	City / State / ZIP / Country	
	Telephone: ()	FAX: ()
Appli	cation (optional):	
Wou	ld you like a reply?YN	
Devi	ce: MCP6141/2/3/4 Liter	rature Number: DS21668A
Ques	stions:	
1. V	What are the best features of this doc	ument?
_		
_		
2. H	low does this document meet your h	ardware and software development needs?
_		
_		
3. E	Do you find the organization of this do	ocument easy to follow? If not, why?
_		
_		
4. V	What additions to the document do yc	ou think would enhance the structure and subject?
_		
_		
5. V	What deletions from the document co	uld be made without affecting the overall usefulness?
_		
_		
6. I	s there any incorrect or misleading in	formation (what and where)?
_		
7. H	low would you improve this documer	nt?
_		

# **PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	<u>x /xx</u>	Examples:
Device	Temperature Package Range	<ul> <li>a) MCP6141-I/P: Industrial temperature, PDIP package.</li> </ul>
Device:	MCP6141:       CMOS Single Op Amp         MCP6141T:       CMOS Single Op Amp         (Tape and Reel for SOIC, MSOP)         MCP6142:       CMOS Dual Op Amp         MCP6142T:       CMOS Dual Op Amp         (Tape and Reel for SOIC and TSSOP)         MCP6143:       CMOS Single Op Amp w/CS Function         MCP6143:       CMOS Single Op Amp w/CS Function         (Tape and Reel for SOIC and MSOP)         MCP6144:       CMOS Quad Op Amp         MCP6144:       CMOS Quad Op Amp         MCP6144:       CMOS Quad Op Amp         MCP6144T:       CMOS Quad Op Amp         MCP6144T:       CMOS Quad Op Amp         MCP6144T:       CMOS Quad Op Amp	<ul> <li>b) MCP6141T-I/SN: Tape and Reel, Industrial temperature, SOIC package.</li> <li>a) MCP6142-I/SN: Industrial temperature, SOIC package.</li> <li>b) MCP6142-I/MS: Industrial temperature, MSOP package.</li> <li>a) MCP6143-I/MS: Industrial temperature, MSOP package.</li> <li>b) MCP6143-I/P: Industrial temperature, PDIP package.</li> </ul>
Temperature Range:	$I = -40^{\circ}C \text{ to } +85^{\circ}C$	a) MCP6144-I/SL: Industrial temperature, SIOC package.
Package:	MS = Plastic MSOP, 8-lead P = Plastic DIP (300 mil Body), 8-lead, 14-lead SN = Plastic SOIC (150 mil Body), 8-lead SL = Plastic SOIC (150 mil Body), 14-lead ST = Plastic TSSOP (4.4mm Body), 14-lead	b) MCP6144T-I/ST: Tape and Reel, Indus- trial temperature, TSSOP package.

#### Sales and Support

#### Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office

- 2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
- 3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

#### New Customer Notification System

Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

NOTES:

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

#### Trademarks

The Microchip name and logo, the Microchip logo, KEELOQ, MPLAB, PIC, PICmicro, PICSTART and PRO MATE are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, microID, MXDEV, MXLAB, PICMASTER, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

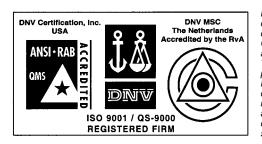
dsPIC, dsPICDEM.net, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, microPort, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, PICC, PICDEM, PICDEM.net, rfPIC, Select Mode and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

Serialized Quick Turn Programming (SQTP) is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2002, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.





Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999 and Mountain View, California in March 2002. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUS, KEEL0Q® code hopping devices, Serial EEPROMs, microperipherals, non-volatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.



# WORLDWIDE SALES AND SERVICE

#### AMERICAS

**Corporate Office** 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: 480-792-7627 Web Address: http://www.microchip.com

#### **Rocky Mountain**

2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7966 Fax: 480-792-4338

#### Atlanta

500 Sugar Mill Road, Suite 200B Atlanta, GA 30350 Tel: 770-640-0034 Fax: 770-640-0307

Boston

2 Lan Drive, Suite 120 Westford, MA 01886 Tel: 978-692-3848 Fax: 978-692-3821

Chicago

333 Pierce Road, Suite 180 Itasca, IL 60143 Tel: 630-285-0071 Fax: 630-285-0075

Dallas

4570 Westgrove Drive, Suite 160 Addison, TX 75001

Tel: 972-818-7423 Fax: 972-818-2924 Detroit

Tri-Atria Office Building 32255 Northwestern Highway, Suite 190 Farmington Hills, MI 48334 Tel: 248-538-2250 Fax: 248-538-2260 Kokomo

2767 S. Albright Road Kokomo, Indiana 46902 Tel: 765-864-8360 Fax: 765-864-8387

Los Angeles

18201 Von Karman, Suite 1090 Irvine, CA 92612 Tel: 949-263-1888 Fax: 949-263-1338

New York

150 Motor Parkway, Suite 202 Hauppauge, NY 11788 Tel: 631-273-5305 Fax: 631-273-5335

San Jose

Microchip Technology Inc. 2107 North First Street, Suite 590 San Jose, CA 95131 Tel: 408-436-7950 Fax: 408-436-7955

Toronto

6285 Northam Drive, Suite 108 Mississauga, Ontario L4V 1X5, Canada Tel: 905-673-0699 Fax: 905-673-6509

#### ASIA/PACIFIC

Australia

Microchip Technology Australia Pty Ltd Suite 22, 41 Rawson Street Epping 2121, NSW Australia

Tel: 61-2-9868-6733 Fax: 61-2-9868-6755 China - Beijing

Microchip Technology Consulting (Shanghai) Co., Ltd., Beijing Liaison Office Unit 915 Bei Hai Wan Tai Bldg. No. 6 Chaoyangmen Beidajie Beijing, 100027, No. China Tel: 86-10-85282100 Fax: 86-10-85282104

#### China - Chengdu

Microchip Technology Consulting (Shanghai) Co., Ltd., Chengdu Liaison Office Rm. 2401, 24th Floor, Ming Xing Financial Tower No. 88 TIDU Street Chengdu 610016, China Tel: 86-28-86766200 Fax: 86-28-86766599

#### China - Fuzhou

Microchip Technology Consulting (Shanghai) Co., Ltd., Fuzhou Liaison Office Unit 28F, World Trade Plaza No. 71 Wusi Road Fuzhou 350001, China Tel: 86-591-7503506 Fax: 86-591-7503521 China - Shanghai

Microchip Technology Consulting (Shanghai) Co., Ltd. Room 701, Bldg. B Far East International Plaza No. 317 Xian Xia Road Shanghai, 200051 Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

#### China - Shenzhen

Microchip Technology Consulting (Shanghai) Co., Ltd., Shenzhen Liaison Office Rm. 1315, 13/F, Shenzhen Kerry Centre, Renminnan Lu Shenzhen 518001, China Tel: 86-755-2350361 Fax: 86-755-2366086

China - Hong Kong SAR

Microchip Technology Hongkong Ltd. Unit 901-6, Tower 2, Metroplaza 223 Hing Fong Road Kwai Fong, N.T., Hong Kong Tel: 852-2401-1200 Fax: 852-2401-3431

#### India

Microchip Technology Inc. India Liaison Office **Divvasree Chambers** 1 Floor, Wing A (A3/A4) No. 11, O'Shaugnessey Road Bangalore, 560 025, India Tel: 91-80-2290061 Fax: 91-80-2290062

#### Japan

Microchip Technology Japan K.K. Benex S-1 6F 3-18-20, Shinyokohama Kohoku-Ku, Yokohama-shi Kanagawa, 222-0033, Japan Tel: 81-45-471- 6166 Fax: 81-45-471-6122 Korea Microchip Technology Korea 168-1, Youngbo Bldg. 3 Floor Samsung-Dong, Kangnam-Ku Seoul, Korea 135-882 Tel: 82-2-554-7200 Fax: 82-2-558-5934 Singapore Microchip Technology Singapore Pte Ltd. 200 Middle Road #07-02 Prime Centre Singapore, 188980 Tel: 65-6334-8870 Fax: 65-6334-8850 Taiwan Microchip Technology (Barbados) Inc., Taiwan Branch 11F-3, No. 207 Tung Hua North Road Taipei, 105, Taiwan Tel: 886-2-2717-7175 Fax: 886-2-2545-0139 EUROPE

#### Austria

Microchip Technology Austria GmbH Durisolstrasse 2 A-4600 Wels Austria Tel: 43-7242-2244-399 Fax: 43-7242-2244-393 Denmark Microchip Technology Nordic ApS Regus Business Centre Lautrup hoj 1-3 Ballerup DK-2750 Denmark Tel: 45 4420 9895 Fax: 45 4420 9910 France Microchip Technology SARL Parc d'Activite du Moulin de Massy 43 Rue du Saule Trapu Batiment A - ler Etage 91300 Massy, France Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 Germany Microchip Technology GmbH Steinheilstrasse 10 D-85737 Ismaning, Germany Tel: 49-89-627-144 0 Fax: 49-89-627-144-44 Italy Microchip Technology SRL Centro Direzionale Colleoni Palazzo Taurus 1 V. Le Colleoni 1 20041 Agrate Brianza Milan, Italy Tel: 39-039-65791-1 Fax: 39-039-6899883 United Kingdom Microchip Ltd.

505 Eskdale Road Winnersh Triangle Wokingham Berkshire, England RG41 5TU Tel: 44 118 921 5869 Fax: 44-118 921-5820

08/01/02

# **Mouser Electronics**

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

# Microchip:

MCP6143-E/P MCP6143-I/MS MCP6143-I/SN MCP6144-E/P MCP6143-E/SN MCP6144-I/SL MCP6144-I/ST MCP6141-I/SN MCP6141-I/MS MCP6141T-I/SN MCP6142T-I/MS MCP6144T-I/SL MCP6144T-I/ST MCP6143T-I/SN MCP6141T-I/MS MCP6142T-I/SN MCP6143T-I/MS MCP6142-I/P MCP6142-E/MS MCP6142-E/SN MCP6144-I/P MCP6141-I/P MCP6142-I/SN MCP6143-I/P MCP6144-E/SL MCP6144-E/ST MCP6141-E/MS MCP6141-E/SN MCP6142-E/P MCP6141-E/P MCP6143-E/MS MCP6142-I/MS MCP6142T-E/SN MCP6144T-E/SL MCP6144T-E/ST MCP6141T-E/MS MCP6143T-E/SN MCP6143T-E/MS MCP6141T-E/SN MCP6142T-E/SN MCP6142T-E/MS MCP6142T-E/MSVAO MCP6144T-E/STVAO MCP6142-E/MSVAO