PERFECT WIRELESS EXPERIENCE

FIBOCOM SC820 Series Hardware Guide

Version: V1.0.3

Date: 2020-06-29

Applicability Type

No.	Product Model	Description
1	SC820-CN-00	2GB+16GB eMCP, High-performance 4G version
2	SC820-W-00	High-performance WIFI version ,Only support 2.4G/5G WIFI
3	SC820-CN-20	4GB+64GB eMCP, High-performance 4G version, not support 2/3G DRX

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Change History

Version	Author	Assessor	Approver	Update Date	Description
V1.0.3	Gao TianHuan Liu Qiang	Tu Min Li Xiyi	Chen Guojiang	2020-06-29	Update the time of Power ON/OFF Modify the description of PIN_54 and PIN_55 Update the data of RF power Update the power of BT Add product model of SC820-CN-20
V1.0.2	Gao Ying	Tu Min	Tu Min	2018-07-24	Update figure 24~36 and table 25
V1.0.1	Gu Zhaoqiang	Tu Min	Tu Min	2018-06-08	Update table 18, 20, 21, 23
V1.0.0	Gu Zhaoqiang	Tu Min	Tu Min	2018-05-28	Initial version

Contents

1 Introduction

1.1 Purpose

This document describes the electrical characteristics, RF performance, structure size, application environment, etc. of SC820 series module (hereinafter referred to as module). With the assistance of this document and other related documents, the developers can quickly understand the hardware functions of the module and develop products.

1.2 Reference Standards

The design of the product refers to the following standards:

- *3GPP TS 51.010-1 V10.5.0: Mobile Station (MS) conformance specification; Part 1: Conformance specification*
- *3GPP TS 34.121-1 V10.8.0: User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 1: Conformance specification*
- *3GPP TS 34.122 V10.1.0: Technical Specification Group Radio Access Network; Radio transmission and reception (TDD)*
- *3GPP TS 36.521-1 V10.6.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance testing*
- *3GPP TS 21.111 V10.0.0: USIM and IC card requirements*
- *3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module-Mobile Equipment (SIM-ME) interface*
- *3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module (USIM) application*
- *3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module (USIM) Application Toolkit(USAT)*
- *3GPP TS 36.124V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment*
- *3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)*
- *3GPPTS27.005 V10.0.1: Use of Data Terminal Equipment - Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)*
- *IEEE 802.11n WLAN MAC and PHY, October 2009 + IEEE 802.11-2007 WLAN MAC and PHY, June 2007*
- *IEEE Std 802.11b, IEEE Std 802.11d, IEEE Std 802.11e, IEEE Std 802.11g, IEEE Std 802.11i:*

- *IEEE 802.11-2007 WLAN MAC and PHY, June 2007*
- *Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1+ EDR/3.0/3.0 + HS, August 6, 2009*
- *Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009*

1.3 Related Document

- *FIBOCOM SC820 Series SMT Design Guide*

2 Product Overview

2.1 General Description

The module integrates core components such as Baseband, eMCP, PMU, Transceiver, PA and supports long distance multi-mode communication such as FDD/TDD-LTE, WCDMA, TD-SCDMA, CDMA, CDMA2000-EVDO, GSM, as well as WIFI/BT short-distance radio transmission technology. It supports GNSS wireless positioning technology. The module is embedded with Android operating system and has various interfaces such as MIPI/USB/UART/SPI/I2C. It is the optimal solution for the core system of wireless smart products.

Its corresponding modes and frequency bands are as follows:

Table 2-1 SC820-CN-00/ SC820-CN-20 Support Band

Mode	Band
GSM/GPRS/EDGE	EGSM900/DCS1800
WCDMA	Band 1/8
CDMA/EVDO	BC0
TD-SCDMA	Band 34/39
FDD-LTE	Band 1/3/5/8
TDD-LTE	Band 34/38/39/40/41(2555-2655MHz)
WIFI 802.11a/b/g/n/ac	2402-2482MHz;5180-5825MHz
BT4.2 LE	2402-2480MHz
GNSS	GPS/GLONASS/BeiDou

Table 2-2 SC820-W-00 Support Band (WIFI)

Mode	Band
WIFI 802.11a/b/g/n/ac	2402-2482 MHz; 5180-5825 MHz
BT4.2 LE	2402-2480 MHz

2.2 Main Performance

The module adopts LCC+LGA encapsulation with 232 pins, including 156 LCC pins and 76 LGA pins. The dimension is 43.5mm x 45mm x 2.85mm. It can be embedded in various M2M applications. It is suitable for the development of smart devices such as smart POS, cash registers, robots, UAVs, smart homes, security monitoring and multimedia terminals.

The following table describes the detailed performance parameters of the module.

Table 2-3 Main Performance Parameters

Performance	Description
Power	DC 3.3-4.35V, typical voltage: 3.8V
Application CPU	ARM® CortexTM-A53 8-core 64-bit CPU Up to 2GHz, 4-core 1MB L2 cache+4-core 512KB L2 cache
Memory	2GB LPDDR3+ 16 GB eMMC Flash/ 4GB LPDDR3+ 64 GB eMMC Flash
Power class	Class 4 (33dBm±2dB) for GSM900 Class 1 (30dBm±2dB) for DCS1800 Class E2 (27dBm±3dB) for GSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800 8-PSK Class 3 (24dBm±1dB) for CDMA BC0 Class 3 (24dBm+1/-3dB) for WCDMA bands Class 2 (24dBm+1/-3dB) for TD-SCDMA bands Class 3 (23dBm±2dB) for LTE FDD bands Class 3 (23dBm±2dB) for LTE TDD bands
GSM/GPRS/EDGE features	R99: ● CSD transmission rate: 9.6kbps, 14.4kbps GPRS: ● Support GPRS multi-slot class 33 ● Coding formats: CS-1/CS-2/CS-3 and CS-4 ● 5 Rx time slots per frame maximum EDGE: ● Support EDGE multi-slot class 33 ● Support GMSK and 8-PSK ● Uplink encoding format: CS 1-4 and MCS 1-9 ● Downlink encoding format: CS 1-4 and MCS 1-9
WCDMA features	Support 3GPP R8 DC-HSPA+ Support 16-QAM, 64-QAM and QPSK modulation CAT6 HSUPA: Maximum uplink rate 5.76Mbps CAT24 DC-HSPA+: Maximum downlink rate 42Mbps

Performance	Description
CDMA/EVDO features	Support CDMA 1X Advanced, 1XEV-DOr0/-DOrA Maximum uplink rate 1.8Mbps, maximum downlink rate 3.1Mbps
TD-SCDMA features	Support CCSA Release 4 Maximum uplink rate 2.2Mbps, maximum downlink rate 4.2Mbps
LTE features	Support FDD/TDD CAT4 Support 1.4-20M RF bandwidth Downlink support 2 × 2 MIMO Maximum uplink rate 50Mbps, maximum downlink rate 150Mbps
WLAN features	Support 2.4G and 5G WLAN wireless communication Support 802.11a, 802.11b, 802.11g, 802.11n and 802.11ac Up to 433Mbps
Bluetooth features	BT4.2 (BR/EDR+BLE)
Satellite positioning	GPS/GLONASS/BeiDou
SMS	Text and PDU modes Point-to-Point MO and MT SMS cell broadcast SMS storage: stored in the module by default
LCD interface	Two 4-Lane MIPI_DSI interfaces Support FHD (1920 × 1200) 60 fps Support dual-screen display (synchronous display or asynchronous display)
Camera interface	One 4-Lane MIPI_CSI interface + one 2-Lane MIPI_CSI interface Up to 2.1Gbps per lane Support 2 cameras Supports up to 24MP pixels
Audio interface	Audio Input: 2 analog microphone inputs Integrated internal bias Audio output: Class AB stereo headphone output Class AB differential handset output Class D differential speaker amplifier output LINEOUT differential audio output
USB interface	One USB2.0 HS interface, with data transfer rate up to 480 Mbps One USB3.0 SS interface, with data transfer rate up to 5Gbps

Performance	Description
	Support USB Type-C interface Support USB OTG (an additional 5V power supply chip is required if there is no PMI8952 power management chip inside the module)
SIM interface	Two USIM card interfaces supporting USIM/SIM card: 1.8/3V adaptive Support dual sim dual standby (default single)
UART interface	Three UART serial interfaces, One 4-lane serial interface supporting RTS and CTS hardware flow , with the maximum rate up to 4Mbps Two 2-lane serial interfaces
SD interface	Support SD3.0, 4bit SDIO; SD card supports hot plug
I2C interface	Multiple I2C interfaces, and can be used for peripherals such as TP, Camera, and Sensor
ADC interface	One-lane universal 15bits ADC
RTC	Support
Antenna interface	MAIN antenna, DRX antenna, GNSS antenna, WIFI/BT antenna interface
Physical characteristics	Dimension: 43.5mm * 45mm * 2.85mm Encapsulation: 156 LCC pin + 76 LGA pin Weight: 12.3±1g
Temperature range	Operating temperature: -25°C - 75°C [1)] Storage temperature: -40°C - 85°C
Software update	USB/OTA/SD
RoHS	RoHS Compliant

Note:

When the module is operating in this temperature range, the functions of it are normal and the relevant performance meets the 3GPP standard.

2.3 Hardware Diagram

The following hardware diagram shows the main hardware functions of the module, including the following ones:

- Baseband
- Wireless transceiver
- PMU
- Storage
- Peripheral interface

-- Communication expansion interface (USB/UART/I2C/SDIO/SPI)

--USIM card interface

--MIPI DSI interface

--MIPI CSI interface

-- Analog audio interface

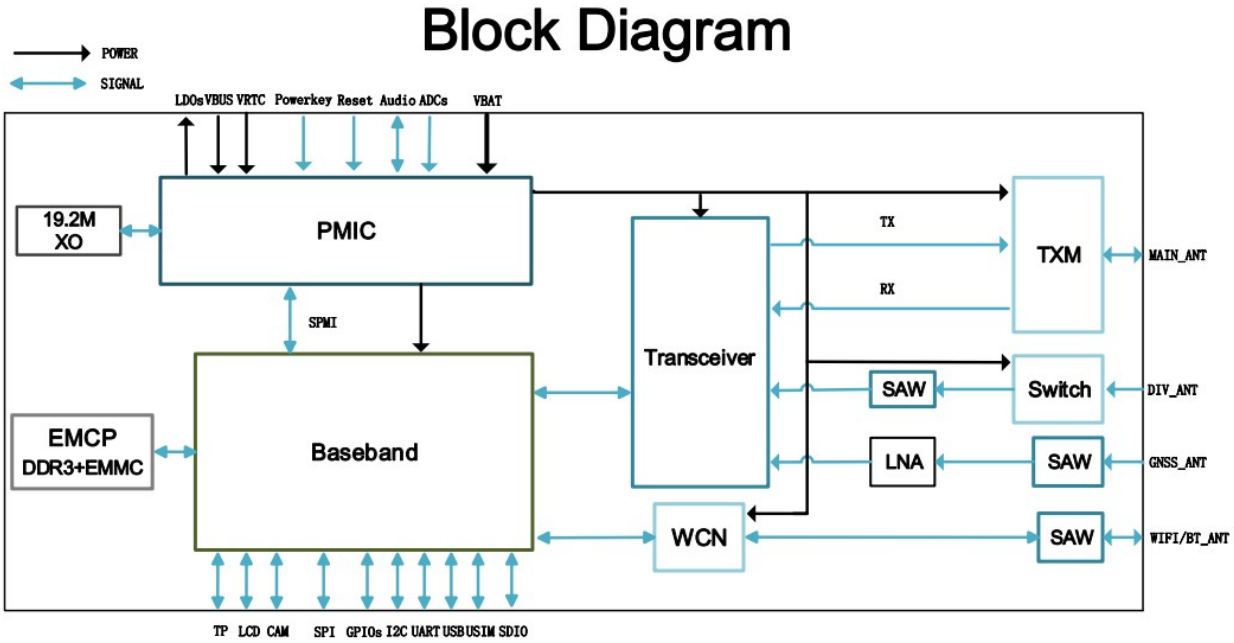

Figure 2-1 Hardware Block Diagram

2.4 Pin Description

2.4.1 Pin Distribution

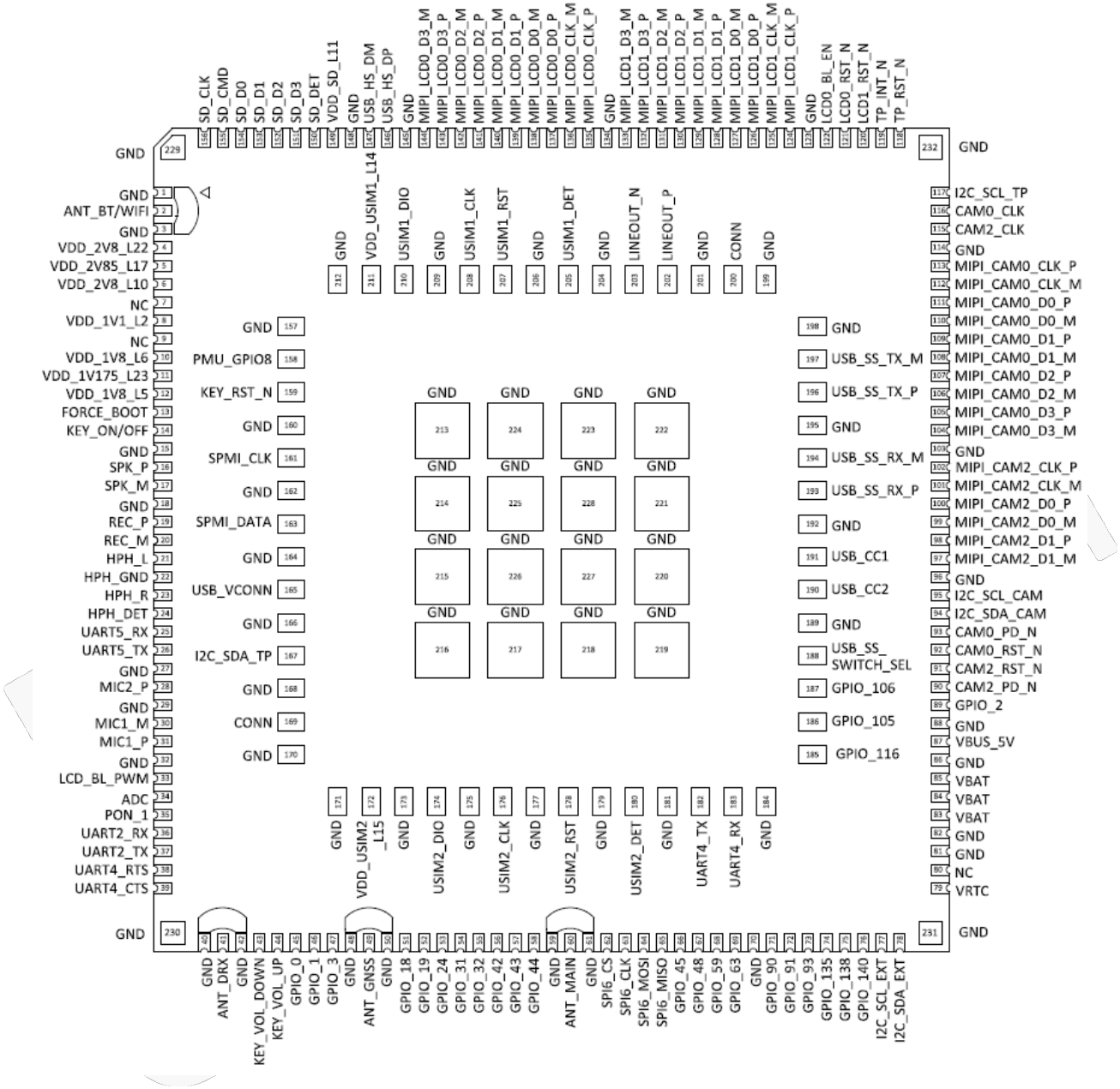

Figure 2-2 Pin Distribution (TOP perspective)

Note:

The pin “NC” stands for No Connect, the pin for this position is reserved and does not need to be connected.

2.4.2 Pin Definition

Table 2-4 I/O Parameter Definition

Type	Description
IO	Input/output
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
OD	Open drain

The module's pin functions and electrical characteristics are described in the following table:

Table 2-5 Pin Description

Pin Name	Pin No.	I/O	Pin Description	Note
Power				
VBAT	83,84,85	PI	Main power input	-
VRTC	79	PI/PO	RTC clock power supply pin	-
VDD_1V1_L2	8	PO	1.1V voltage output	-
VDD_1V8_L5	12	PO	1.8V voltage output	-
VDD_1V8_L6	10	PO	1.8V voltage output	-
VDD_2V8_L10	6	PO	2.8V voltage output	-
VDD_SD_L11	149	PO	SD card power supply, 2.95V	-
VDD_USIM1_L14	211	PO	SIM card 1 power supply	1.8/3 V adaptive
VDD_ USIM2_L15	172	PO	SIM card 2 power supply	1.8/3 V adaptive

Pin Name	Pin No.	I/O	Pin Description	Note
VDD_2V85_L17	5	PO	2.85V voltage output	-
VDD_2V8_L22	4	PO	2.8V voltage output	-
VDD_1V175_L23	11	PO	1.175V voltage output	-
GND	1,3,15,18,27,29,32,40,42,48,50,59,61,70,81,82,86,88,96,103,114,123,134,145,148,157,160,162,164,166,168,170,171,173,175,177,179,181,184,189,192,195,198,199,201,204,206,209,212,213,214,215,216,217,218,219,220,221,222,223,224,225,226,227,228,229,230,231,232		Ground	69
Button				
KEY_ON/OFF	14	DI	Power switch	Active low
KEY_VOL_UP	44	DI	Volume +	Active low
KEY_VOL_DOWN	43	DI	Volume -	Active low
SIM card interface				
USIM1_DIO	210	I/O	SIM card 1 data signal	-
USIM1_CLK	208	DO	SIM card 1 clock signal	-
USIM1_RST	207	DO	SIM card 1 reset signal	-

Pin Name	Pin No.	I/O	Pin Description	Note
USIM1_ DET	205	DI	SIM card 1 plug detection pin	Default disabled
USIM2_DIO	174	I/O	SIM card 2 data signal	-
USIM2_CLK	176	DO	SIM card 2 clock signal	-
USIM2_RST	178	DO	SIM card 2 reset signal	-
USIM2_ DET	180	DI	SIM card 2 plug detection pin	Default disabled
SD card interface				
SD_D3	151	I/O	SD card data interface	-
SD_D2	152	I/O	SD card data interface	-
SD_D1	153	I/O	SD card data interface	-
SD_D0	154	I/O	SD card data interface	-
SD_CLK	156	DO	SD card clock	-
SD_CMD	155	I/O	SD card command interface	-
SD_DET	150	DI	SD card detection	Active low
I2C interface				
I2C_SCL_EXT	77	OD	sensor I2C clock	-
I2C_SDA_EXT	78	OD	sensor I2C data cable	-
I2C_SCL_TP	117	OD	TP I2C clock	-
I2C_SDA_TP	167	OD	TP I2C data cable	-

Pin Name	Pin No.	I/O	Pin Description	Note
I2C_SCL_CAM	95	OD	camera I2C clock	Can't use as other I2C and GPIO
I2C_SDA_CAM	94	OD	camera I2C data cable	
USB interface				
VBUS_5V	87	PI	Device mode, 5V input	Only for USB detection signal
USB_HS_DP	146	I/O	USB 2.0 differential data signal	-
USB_HS_DM	147	I/O		-
USB_SS_RX_P	193	DI	USB 3.0 differential data reception signal	-
USB_SS_RX_M	194	DI		-
USB_SS_TX_P	196	DO	USB 3.0 differential data transmission signal	-
USB_SS_TX_M	197	DO		-
USB_CC1	191	I/O	USB Type-C connector configuration pin	-
USB_CC2	190	I/O		-
USB_SS_SWITCH_SEL	188	DO	USB Type-C data switch control	-
USB_VCONN	165	AI	Power input (5V, 210mA), is used to drive the Active data cable	1) When 5V is taken directly from VBUS_5V, OVP protection device needs to be added; 2) Internally connected to CC1 or CC2 via a multiplexer (depending on the insertion direction of Type-C data cable);
UART interface				
UART2_TX	37	DO	UART2 data transmission	Debug serial interface default
UART2_RX	36	DI	UART2 data reception	

Pin Name	Pin No.	I/O	Pin Description	Note
UART4_TX	182	DO	UART4 data transmission	-
UART4_RX	183	DI	UART4 data reception	-
UART4_CTS	39	DI	UART4 clear to send	-
UART4_RTS	38	DO	UART4 request to send	-
UART5_TX	26	DO	UART5 data transmission	-
UART5_RX	25	DI	UART5 data reception	-
SPI interface				
SPI6_CLK	63	I/O	SPI6 clock	Only support master mode, don't support DMA mode
SPI6_CS	62	I/O	SPI6 chip selection	
SPI6_MOSI	64	I/O	SPI6 data channel; master output, slave input	
SPI6_MISO	65	I/O	SPI6 data channel; master input, slave output	
LCD interface				
MIPI_LCD0_CLK_P	135	AO	LCD0 MIPI differential clock signal	-
MIPI_LCD0_CLK_M	136	AO		-
MIPI_LCD0_D0_P	137	AI/AO	LCD0 MIPI differential data signal	-
MIPI_LCD0_D0_M	138	AI/AO		-
MIPI_LCD0_D1_P	139	AI/AO		-
MIPI_LCD0_D1_M	140	AI/AO		-

Pin Name	Pin No.	I/O	Pin Description	Note
MIPI_LCD0_D2_P	141	AI/AO		-
MIPI_LCD0_D2_M	142	AI/AO		-
MIPI_LCD0_D3_P	143	AI/AO		-
MIPI_LCD0_D3_M	144	AI/AO		-
LCD0_RST_N	121	DO	LCD0 reset signal	-
MIPI_LCD1_CLK_P	124	AO	LCD1 MIPI differential clock signal	-
MIPI_LCD1_CLK_M	125	AO		-
MIPI_LCD1_D0_P	126	AI/AO	LCD1 MIPI differential data signal	-
MIPI_LCD1_D0_M	127	AI/AO		-
MIPI_LCD1_D1_P	128	AI/AO		-
MIPI_LCD1_D1_M	129	AI/AO		-
MIPI_LCD1_D2_P	130	AI/AO		-
MIPI_LCD1_D2_M	131	AI/AO		-
MIPI_LCD1_D3_P	132	AI/AO		-
MIPI_LCD1_D3_M	133	AI/AO		-
LCD1_RST_N	120	DO	LCD1 reset signal, Active low	-
LCD_BL_PWM	33	DO	LCD backlight PWM control signal	-
LCD0_BL_EN	122	DO	LCD backlight enable control signal	-
Camera interface				
MIPI_CAM0_CLK_P	113	AI	CAM0 MIPI differential clock signal	-
MIPI_CAM0_CLK_M	112	AI		-

Pin Name	Pin No.	I/O	Pin Description	Note
MIPI_CAM0_D0_P	111	AI/AO	CAM0 MIPI differential data signal	-
MIPI_CAM0_D0_M	110	AI/AO		-
MIPI_CAM0_D1_P	109	AI/AO		-
MIPI_CAM0_D1_M	108	AI/AO		-
MIPI_CAM0_D2_P	107	AI/AO		-
MIPI_CAM0_D2_M	106	AI/AO		-
MIPI_CAM0_D3_P	105	AI/AO		-
MIPI_CAM0_D3_M	104	AI/AO		-
CAM0_CLK	116	DO	CAM0 main clock signal	-
CAM0_RST_N	92	DO	CAM0 reset signal	-
CAM0_PD_N	93	DO	CAM0 shutdown signal	-
MIPI_CAM2_CLK_P	102	AI	CAM2 MIPI differential clock signal	-
MIPI_CAM2_CLK_M	101	AI		-
MIPI_CAM2_D0_P	100	AI/AO	CAM2 MIPI differential data signal	-
MIPI_CAM2_D0_M	99	AI/AO		-
MIPI_CAM2_D1_P	98	AI/AO		-
MIPI_CAM2_D1_M	97	AI/AO		-
CAM2_CLK	115	DO	CAM2 main clock signal	-
CAM2_RST_N	91	DO	CAM2 reset signal	-
CAM2_PD_N	90	DO	CAM2 shutdown signal	--
Touch panel interface				

Pin Name	Pin No.	I/O	Pin Description	Note
TP_INT_N	119	DI	TP interrupt signal	-
TP_RST_N	118	DO	TP reset signal	-
Audio interface				
SPK_P	16	AO	Class D amplifier differential output	-
SPK_M	17	AO		-
REC_P	19	AO	Receiver differential output	-
REC_M	20	AO		-
HPH_L	21	AO	Headphone left channel output	-
HPH_GND	22	/	Headphone ground	-
HPH_R	23	AO	Headphone right channel output	-
HPH_DET	24	AI	Headphone plug detection	-
MIC2_P	28	AI	Headphone MIC input	-
MIC1_M	30	AI	Main MIC differential input -	-
MIC1_P	31	AI	Main MIC differential input +	-
LINEOUT_P	202	AO	Audio Lineout differential output	-
LINEOUT_M	203	AO		-
Antenna interface				
ANT_MAIN	60	I/O	2G/3G/4G main antenna	-
ANT_DRX	41	AI	Diversity reception antenna	-

Pin Name	Pin No.	I/O	Pin Description	Note
ANT_BT/WIFI	2	I/O	WIFI/BT antenna	-
ANT_GNSS	49	AI	GNSS antenna	-
Other interfaces				
FORCE_BOOT	13	DI	Forced download pin	Active high
ADC	34	AI	ADC detection pin	0~1.7V or 0.3~VBAT Configurable
PON_1	35	DI	Power on pin	Power on trigger by high level, connect PMI8952's PGOOD_SYSOK pin when use PMI8952
SPMI_CLK	161	DO	SPMI interface	Connect PMI8952's SPMI interface when use PMI8952
SPMI_DATA	163	I/O		
KEY_RST_N	159	DO	Reset	use for PMI8952
GPIO interface				
GPIO_0	45	I/O	Ordinary GPIO, 1.8V power domain	B-PD:nppukp
GPIO_1	46	I/O		B-PD:nppukp
GPIO_2	89	I/O		B-PD:nppukp
GPIO_3	47	I/O		B-PD:nppukp
GPIO_18	51	I/O		B-PD:nppukp
GPIO_19	52	I/O		B-PD:nppukp
GPIO_24	53	I/O		B-PD:nppukp
GPIO_45	66	I/O		B-PD:nppukp
GPIO_48	67	I/O		B-PD:nppukp
GPIO_59	68	I/O		B-PD:nppukp

Pin Name	Pin No.	I/O	Pin Description	Note
GPIO_63	69	I/O		B-PD:nppukp
GPIO_90	71	I/O		B-PD:nppukp
GPIO_91	72	I/O		B-PD:nppukp
GPIO_93	73	I/O		B-PD:nppukp
GPIO_105	186	I/O		B-PD:nppukp
GPIO_106	187	I/O		B-PD:nppukp
GPIO_116	185	I/O		B-PD:nppukp
GPIO_135	74	I/O		B-PD:nppukp
GPIO_138	75	I/O		B-PD:nppukp
GPIO_140	76	I/O		B-PD:nppukp
GPIO_42	56	I/O		B-PD: nppukp, default configuration as acceleration sensor interrupt input
GPIO_43	57	I/O		B-PD:nppukp, default configuration as light sensor & distance sensor interrupt input
GPIO_44	58	I/O		B-PD: nppukp, default configuration as geomagnetic sensor interrupt input
PMU_GPIO_8	158	I/O	PM8953's GPIO	-
Reserved pin				
NC	7,9,54,55,80		Reserved pin	No connection
CONN	169,200		Reserved pin	Two pins are short inside the module

3 Application Interface

3.1 Power

The module provides three VBAT pins for connecting to external power supply. The input range of power is 3.5V~4.35V and the recommended value is 3.8V. The performance of the power supply to VBAT, such as its load capacity, ripple etc. will directly affect the performance and stability of the module. In extreme cases, the peak current of the module can reach 3A and if the power supply capacity is insufficient, the voltage will drop. If the power voltage instantaneous drop below 3V, the module may be powered off or restarted.

3.1.1 Power Supply

The module is powered by the VBAT pin.

Table 3-1 Power Supply Parameters

Parameters	Minimum Value	Recommended Value	Maximum Value	Unit
VBAT (DC)	3.5	3.8	4.35	V

Power design is shown as follows:

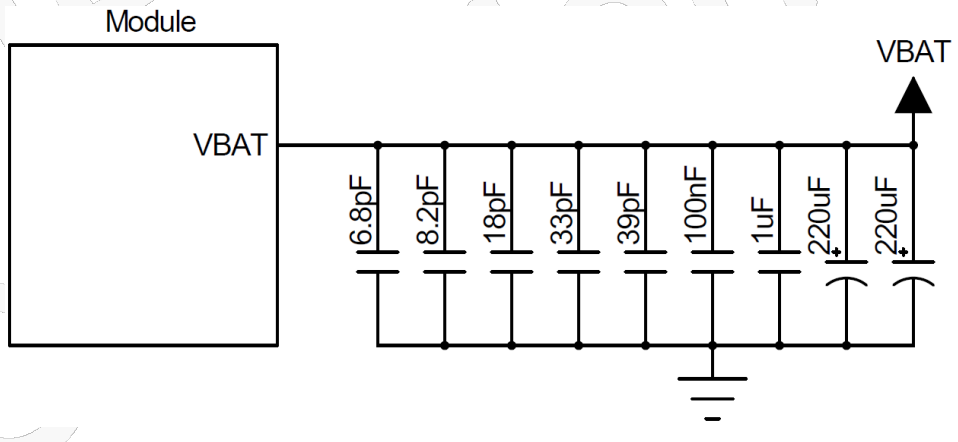

Figure 3-1 Power Design

Power supply decoupling capacitor design is shown in the following table:

Table 3-2 Power Supply Decoupling Capacitor Design

Recommended capacitor	Application	Description
220uF x 2	Voltage stabilizing capacitor	To reduce power fluctuations during module operation, it is required to adopt low ESR capacitor

Recommended capacitor	Application	Description
		LDO or DCDC power requires not less than 440uF capacitor Battery power can be properly reduced to 100 ~ 220uF capacitor
1uF,100nF	Filter capacitor	Filter clock and digital signal interference
39pF,33pF,18pF, 8.2pF,6.8pF	Decoupling capacitor	Filter high frequency interference

The power voltage drop example is shown in the figure:

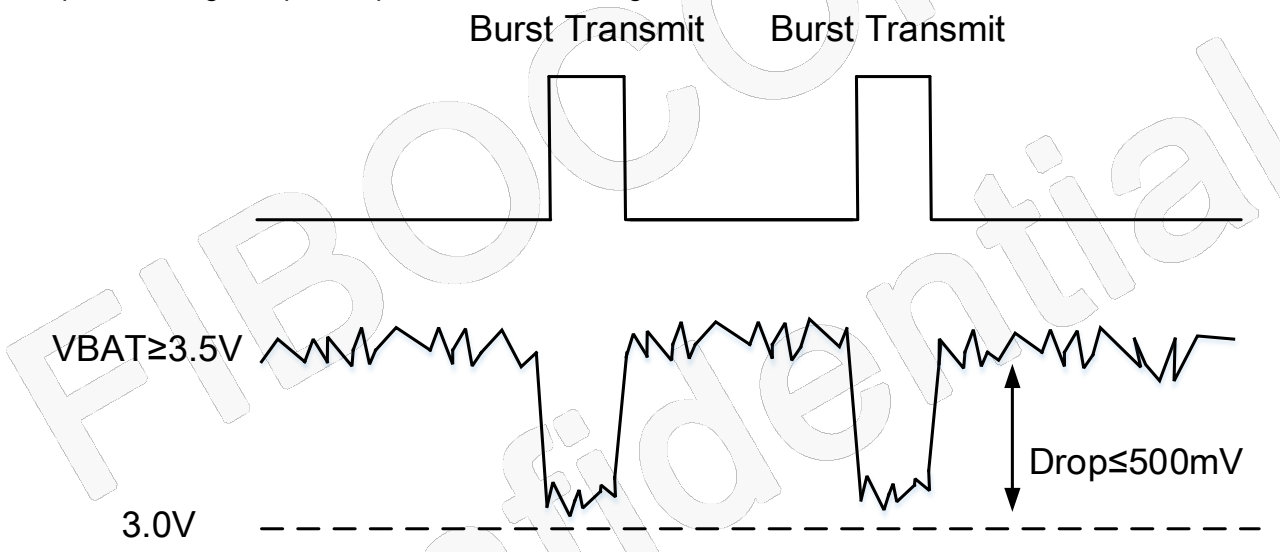

Figure 3-2 Power Voltage Drop Example

To ensure that the power voltage is not lower than 3V, it is recommended to connect two 220μF tantalum capacitors with low ESR and decoupling capacitors of 1uF, 100nF, 39pF and 33pF in parallel to the VBAT input of the module. Besides the PCB trace of VBAT should as short and wide as possible. Reduce the equivalent impedance of the VBAT trace to ensure that at maximum transmit power, significant voltage drop will not occur at high currents. It is recommended that the width of VBAT trace should not be less than 3mm and the ground plane of the power section should be flat.

3.1.2 RTC Power

VRTC is the power supply for the internal RTC clock of the module and can be used as a backup power for it. When the module power VBAT is powered on, the VRTC will output voltage. When there is no VBAT, it needs to be powered by the external power. The button battery is generally used for power supply. The

VRTC parameters are as follows:

Table 3-3 VRTC Parameters

Parameters	Minimum	Typical	Maximum	Unit
VRTC output voltage	2.5	3.1	3.2	V
VRTC input voltage (clock works well)	2.0	3.0	3.25	V
VRTC input current (clock works well)	-	5	-	uA

The reference design circuit of VRTC as RTC clock backup power is shown as follows:

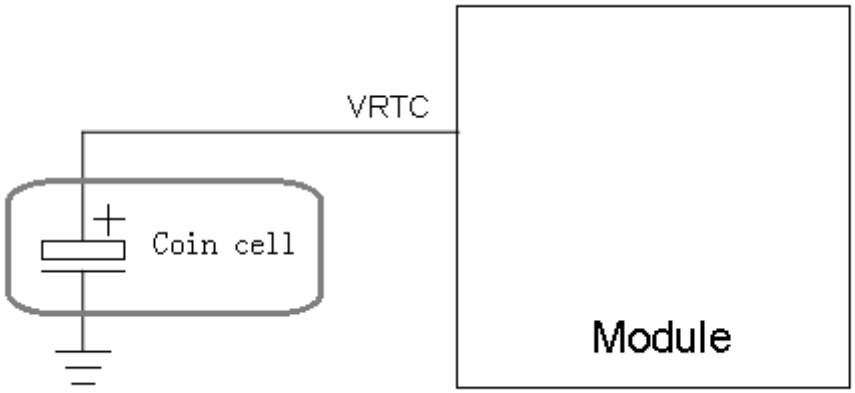

Figure 3-3 VRTC Reference Design Circuit

3.1.3 Power Output

The module has multiple power outputs for peripheral circuits.

33pF and 10pF capacitors can be connected in parallel to avoid high frequency interference effectively.

Table 3-4 Power Description

Pin Name	Programmable Range (V)	Default Voltage (V)	Drive Current (mA)
VDD_1V8_L5	-	1.8	200
VDD_1V8_L6	-	1.8	200
VDD_2V85_L17	1.75~3.3375	2.85	300
VDD_2V8_L22	1.75~3.3375	2.8	150
VDD_1V175_L23	0.375~1.5375	1.1	600

Pin Name	Programmable Range (V)	Default Voltage (V)	Drive Current (mA)
VDD_2V8_L10	1.75~3.3375	2.8	150
VDD_1V1_L2	0.375~1.5375	1.1	1200
VDD_SD_L11	1.75~3.3375	2.95	800
VDD_USIM1_L14	1.75~3.3375	1.8/3	50
VDD_ USIM2_L15	1.75~3.3375	1.8/3	50

3.2 Control Signal

The module uses one control signal to implement power on/off, restart, sleep/wakeup operation for the module.

Table 3-5 Power on/off Pin Definition

Pin Name	Pin No.	I/O	Description	Note
KEY_ON/OFF	14	DI	Default high, active low . This pin can be used for power on/off, restart, sleep/wakeup of the module	

3.2.1 Module Power on

After VBAT is powered, pull down KEY_ON/OFF pin for 2s~10s can trigger module power on . The KEY_ON/OFF control reference diagram is as follows:

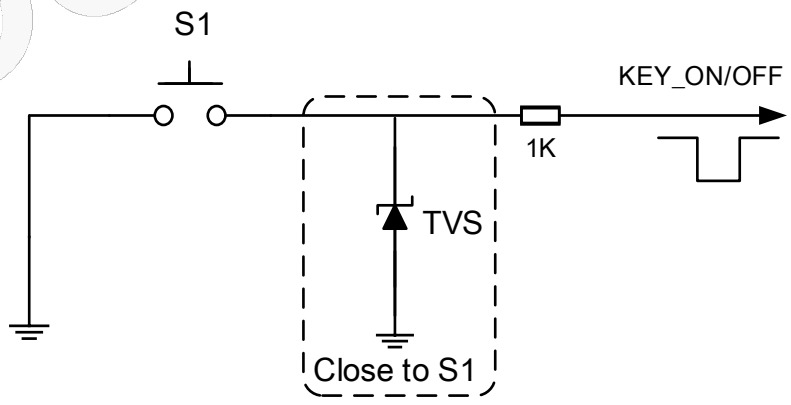

Figure 3-4 Keypad Power on Circuit

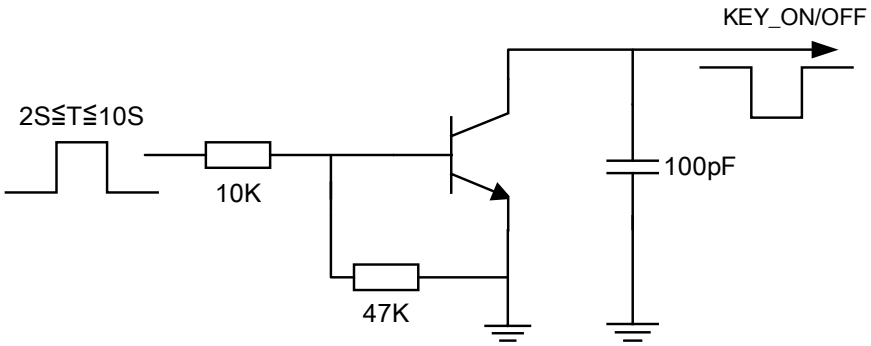

Figure 3-5 Drive Circuit Power on

Power on sequence is shown as follows:

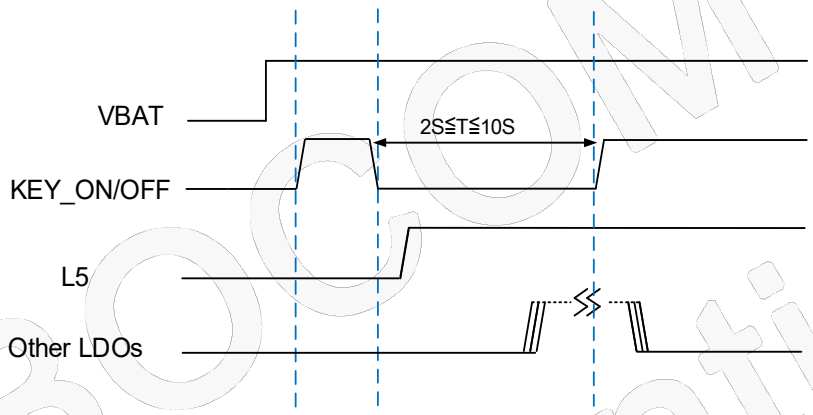

Figure 3-6 Power on Sequence

3.2.2 Module Power down

Normal power off: when module is in operating mode, pull down the KEY_ON/OFF pin for 0.6s and then release it, the display interface will pop up a selection box (select power off or restart).

Force power off: when module is in operating mode, pull down the KEY_ON/OFF pin for 10.5s ~15s the system will be forced to power off. Power off sequence is shown as follows:

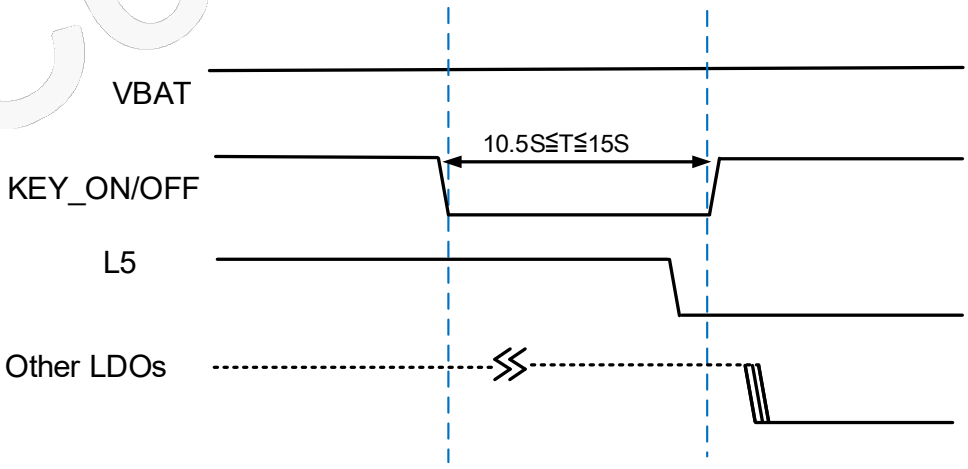

Figure 3-7 Forced Power off Sequence

3.2.3 Sleep/Wakeup

During standby, pull down the KEY_ON/OFF for 0.1s and the system will enter sleep state. The system supports automatic sleep. The time from standby to sleep can be configured via software.

In sleep mode, pulling down the KEY_ON/OFF for 0.1s can wake up the system.

3.2.4 Reset

KEY_VOL_DOWN and KEY_ ON/OFF can use as reset signal, The function and the time of reset can be configured via software.

3.2.5 Volume Keypad

KEY_VOL_DOWN and KEY_VOL_UP are the volume down and volume up keypads; refer to the power on keypad circuit for design of keypad circuit.

3.3 USB Interface

The module supports one USB interface, support for USB3.0 and downward compatibility with USB2.0; USB2.0 supports FS (12Mbps), HS (480Mbps) modes. USB3.0 supports SS (5Gbps) mode. USB supports OTG function (additional 5V power supply is required), HUB expansion interface and type-c interface.

USB pin definition is shown in the following table:

Table 3-6 USB2.0 Pin Definition

Pin Name	Pin No.	I/O	Description	Note
VBUS_5V	87	PI	Device mode, 5V input	-
USB_DM	147	I/O	USB differential signal	-
USB_DP	146	I/O		-

Table 3-7 USB3.0 Pin Definition

Pin Name	Pin No.	I/O	Description	Note
USB_VCONN	165	AI	Power input (5v, 210mA) for driving Active data cable	-

Pin Name	Pin No.	I/O	Description	Note
USB_SS_SWITCH_SEL	188	DO	USB Type-C data switch control	-
USB_SS_RX_P	193	DI	USB 3.0 differential data receiving signal	-
USB_SS_RX_M	194	DI		-
USB_SS_TX_P	196	DO	USB 3.0 differential data transmission signal	-
USB_SS_TX_M	197	DO		-
USB_CC1	191	I/O	USB Type-C connector configuration pin	-
USB_CC2	190	I/O		-

The following figure shows the USB2.0 interface circuit design:

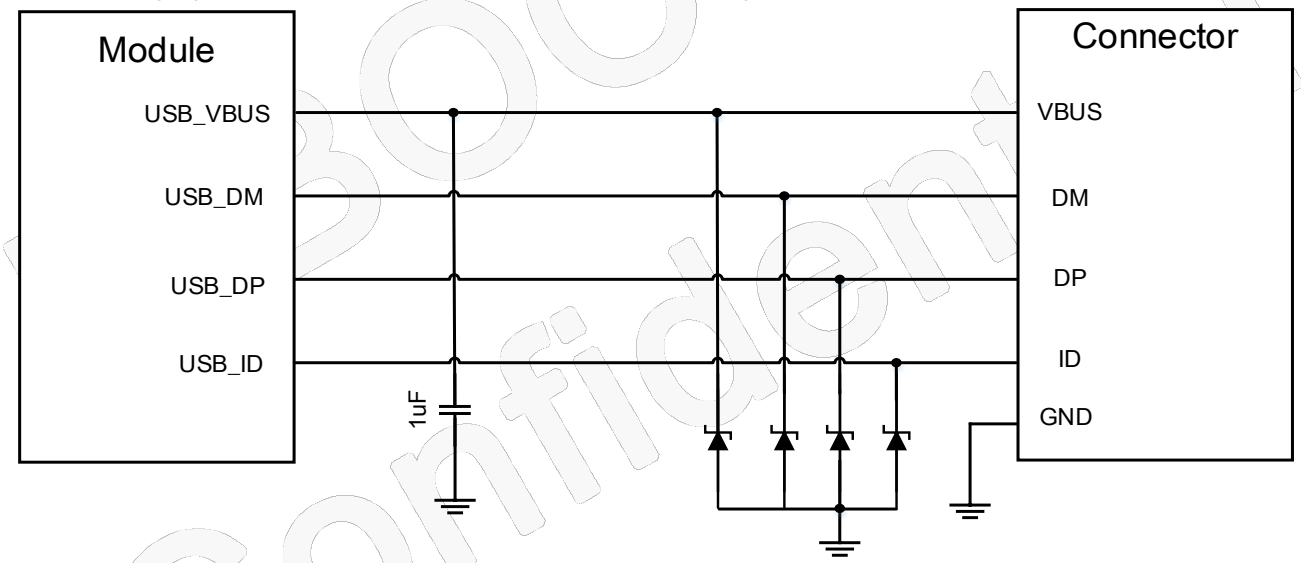

Figure 3-8 USB2.0 Interface Circuit Diagram

Note:

1) The module cannot output 5V DC internally and 5V DC is required when USB is used as a HOST.

2) The total component parasitic capacitance on the USB2.0 differential signal line cannot exceed 2.0pF

3) USB_DP and USB_DM are high-speed differential signal. The highest transmission rate is 480Mbps. Please pay attention to the following requirements in PCB layout:

- USB_DP and USB_DM signal cables are required to be parallel and equal in length (differential cable length controlled within 2mm), while the right-angle route shall be avoided,

and differential 90Ω impedance shall be controlled.

- USB2.0 differential signal cable is laid on the signal layer nearest to the ground, with well grounded
- USB_ID can be simulated by using GPIO, default GPIO_140.

The following figure shows the USB3.0 (type-c) interface circuit design:

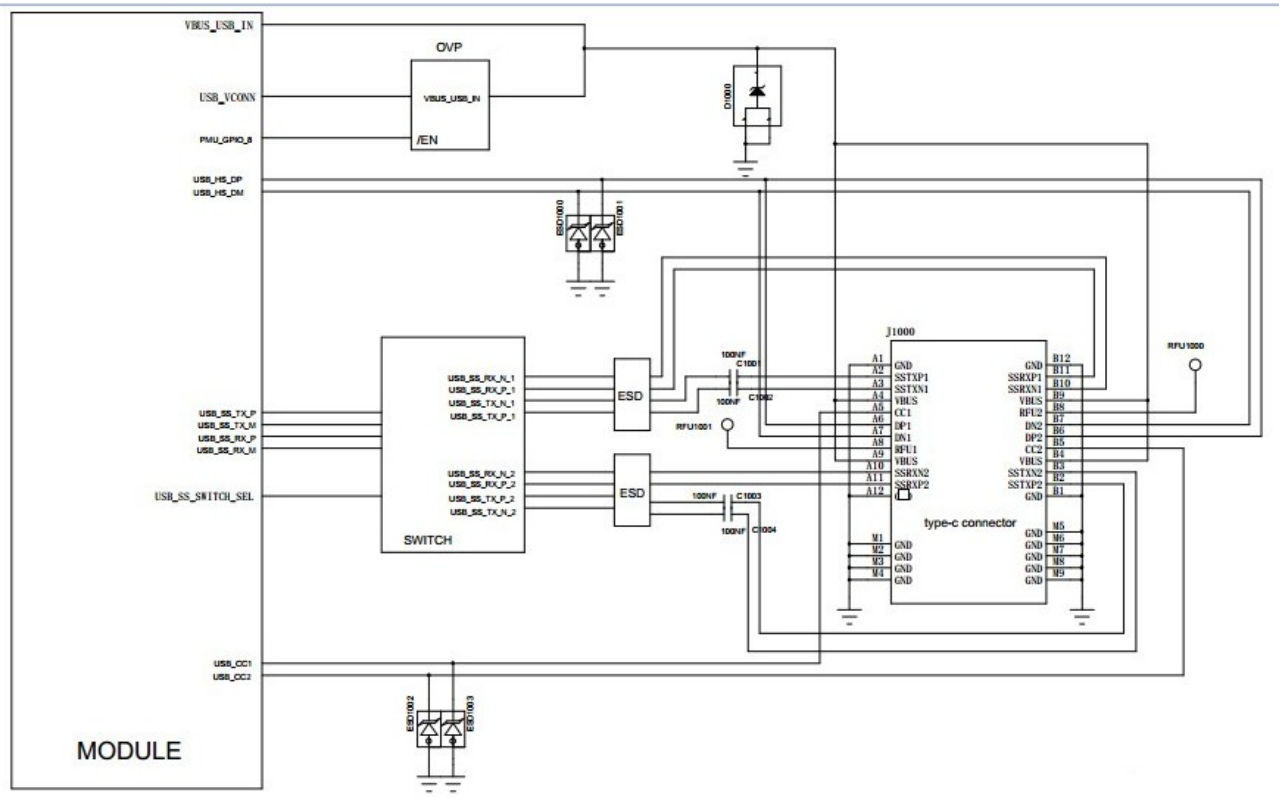

Figure 3-9 USB3.0 (TYPE-C) Interface Circuit Diagram

Note:

1) USB3.0 is a high-speed signal cable and needs to be well-shielded (differential cable ground wrap), and follows the principle of high-speed differential routing.

2) Do differential impedance control, 90 Ω ±10% and control differential cable length within 0.7mm.

3)The total component parasitic capacitance on the USB3.0 TX / RX differential signal line cannot exceed 0.5pF.

3.4 UART Interface

The module defines three UART interfaces.

The module serial interface is 1.8V level. If the peripheral is at other levels, level shift is required.

Table 3-8 UART Interface Pin Definition

Pin Name	Pin No.	I/O	Description	Note
UART2_TX	37	DO	UART2 data transmission	Debug interface
UART2_RX	36	DI	UART2 data reception	
UART4_TX	182	DO	UART4 data transmission	-
UART4_RX	183	DI	UART4 data reception	-
UART4_CTS	39	DI	UART4 clear to send	-
UART4_RTS	38	DO	UART4 request to send	-
UART5_TX	26	DO	UART5 data transmission	-
UART5_RX	25	DI	UART5 data reception	-

All series ports are 1.8V voltage domain, if the peripheral is other voltage domain, please add level shift .

Level shift reference design is shown as follow figure:

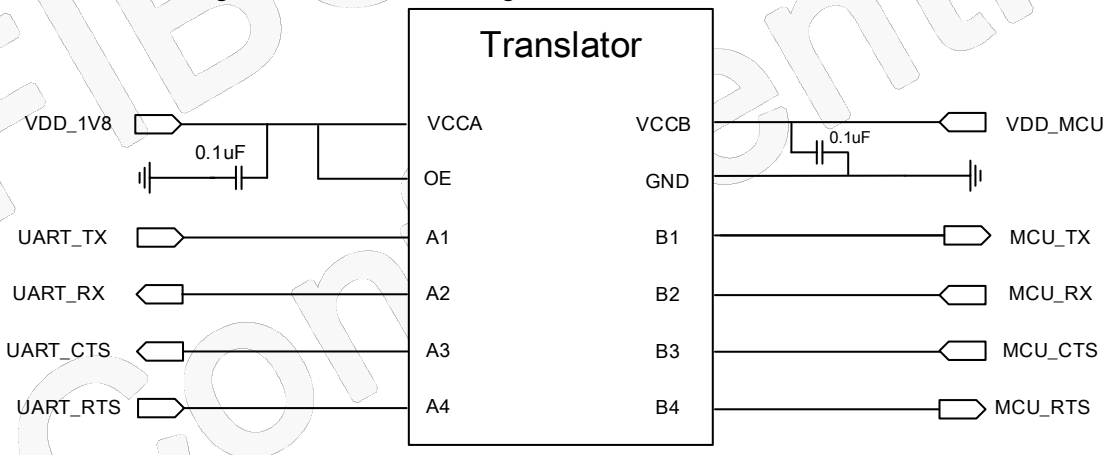

Figure 3-10 Level Shift Reference Design

Note:

Please pay attention to the exchange of the TX and RX, the module TX needs to connect to the PC RX.

3.5 SPI Interface

The module has one SPI interface for use by default but only supports master mode, don't supports DMA

mode.

Table 3-9 SPI Interface Pin Definition

Pin Name	Pin No.	I/O	Description	Note
SPI6_CLK	63	DO	SPI6 clock	-
SPI6_CS	62	DO	SPI6 chip select	-
SPI6_MOSI	64	DO	SPI6 data channel; master output, slave input	-
SPI6_MISO	65	DI	SPI6 data channel; master input, slave output	-

3.6 USIM Interface

The module supports two SIM cards, dual-sim dual-standby single-active (default single) and both support hot plug (default off).

Table 3-10 USIM Pin Definition

Pin Name	Pin No.	I/O	Description	Note
USIM1_DIO	210	I/O	SIM 1 data signal	-
USIM1_CLK	208	DO	SIM 1 clock signal	-
USIM1_RST	207	DO	SIM 1 reset signal	-
USIM1_ DET	205	DI	SIM 1 plug detection pin	-
USIM2_DIO	174	I/O	SIM 2 data signal	-
USIM2_CLK	176	DO	SIM 2 clock signal	-
USIM2_RST	178	DO	SIM 2 reset signal	-
USIM2_ DET	180	DI	SIM 2 plug detection pin	-
VDD_USIM1_L14	211	PO	SIM 1 power supply	-
VDD_ USIM2_L15	172	PO	SIM 2 power supply	-

The reference circuit of USIM card interface is as follows:

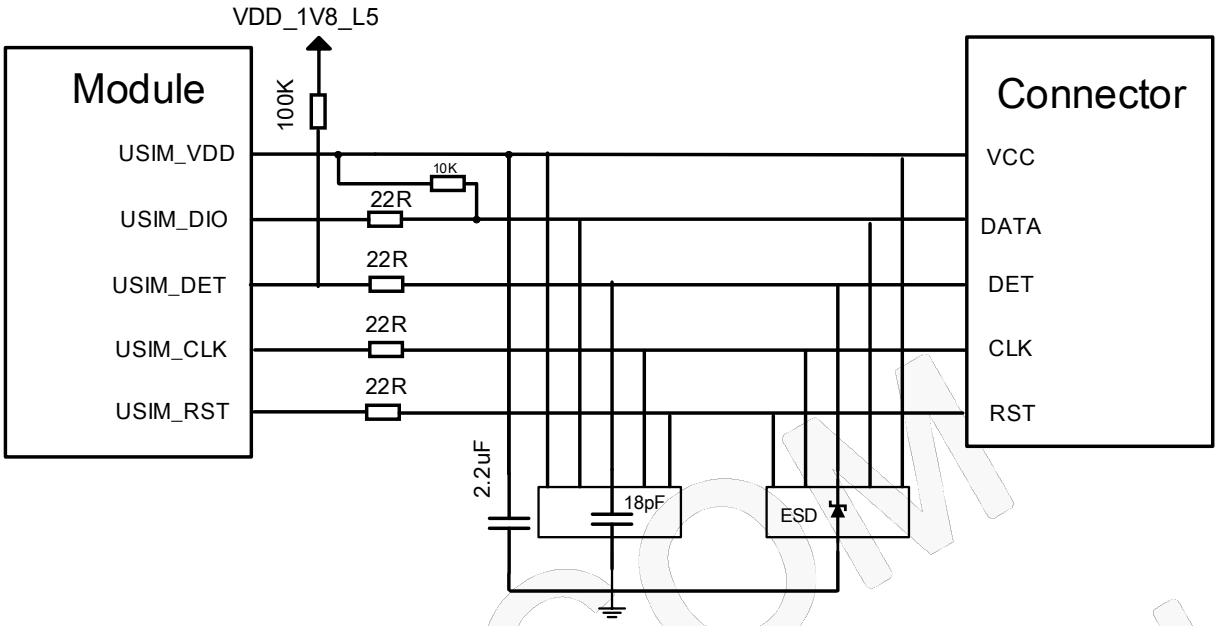

Figure 3-11 Interface Circuit of USIM Card

Note:

1) The length of trace from module to the SIM card holder should be less than 100mm.

2) The layout and routing of the SIM card must be kept away from EMI interference sources such as RF antenna and digital switch signal.

3) The decoupling capacitors of the SIM card signal and the ESD device should be placed close to the card holder.

3.7 SDIO Interface

The module supports one SDIO interface. The pin definition is as follows:

Table 3-11 SDIO Pin Definition

Pin Name	Pin No.	I/O	Description	Note
SD_D3	151	I/O	SD card data interface	-
SD_D2	152	I/O	SD card data interface	-
SD_D1	153	I/O	SD card data interface	-
SD_D0	154	I/O	SD card data interface	-

Pin Name	Pin No.	I/O	Description	Note
SD_CLK	156	DO	SD card clock	-
SD_CMD	155	I/O	SD card command interface	-
SD_DET	150	DI	SD card detection	-
VDD_SD_L11	149	PO	SD power supply	-

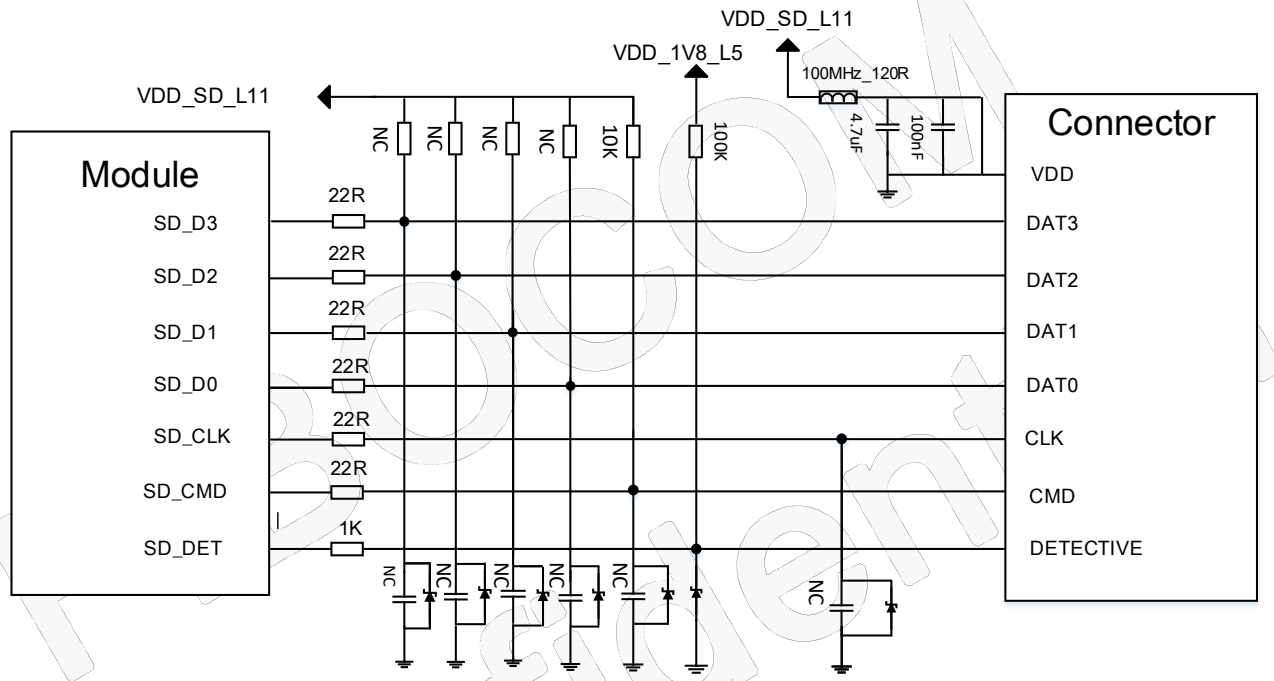

Figure 3-12 SD Card Interface Circuit

Note:

1) VDD_SD_L11 is the SD card peripheral driving power and can provide about 800mA current. controlling the Line width 1MM.

2) Pull up SD_DET with VDD_1V8_L5

3) SDIO is a high-speed digital signal cable, needs to be shielded.

4) SDIO data cable needs to be the same length; The equivalent capacitor must be less than 2pF.

3.8 GPIO Interface

The module has rich GPIO resources and the interface level is 1.8V. The pin definition is as follows:

Table 3-12 GPIO List

Pin Name	Pin No.	Reset Status	Interrupt and Wakeup Function
GPIO_0	45	B-PD	NO
GPIO_1	46	B-PD	YES
GPIO_2	89	B-PD	NO
GPIO_3	47	B-PD	NO
GPIO_18	51	B-PD	NO
GPIO_19	52	B-PD	NO
GPIO_24	53	B-PD	NO
GPIO_45	66	B-PD	YES
GPIO_48	67	B-PD	YES
GPIO_59	68	B-PD	YES
GPIO_63	69	B-PD	YES
GPIO_90	71	B-PD	YES
GPIO_91	72	B-PD	YES
GPIO_93	73	B-PD	YES
GPIO_105	186	B-PD	NO
GPIO_106	187	B-PD	NO
GPIO_116	185	B-PD	NO
GPIO_135	74	B-PD	NO
GPIO_138	75	B-PD	YES
GPIO_140	76	B-PD	YES
GPIO_42	56	B-PD	YES
GPIO_43	57	B-PD	YES
GPIO_44	58	B-PD	YES

Pin Name	Pin No.	Reset Status	Interrupt and Wakeup Function
PMU_GPIO_8	158	B-PD	NO

Note：

B: Bidirectional digital with CMOS input

H: High-voltage tolerant

NP: pdpukp = default no-pull ,with programmable options following the colon (:)

PD: nppukp = default pull down, with programmable options following the colon (:)

PU: nppdkp = default pull up ,with programmable options following the colon (:)

KP: nppdpu = default keeper ,with programmable options following the colon (:)

3.9 I2C Interface

The module provides four I2C interfaces for TP, CAMERA, SENSOR, etc. The four I2C interfaces are all open-drain outputs. When in use, please pull up to 1.8V power domain through pull-up resistors.

Table 3-13 I2C Pin Definition

Pin Name	Pin No.	I/O	Description	Note
I2C_SCL_EXT	77	OD	Sensor I2C clock	-
I2C_SDA_EXT	78	OD	Sensor I2C data	-
I2C_SCL_TP	117	OD	Main TP I2C clock	-
I2C_SDA_TP	167	OD	Main TP I2C data	-
UART4_CTS	39	OD	Sub TP I2C data	GPIO_14
UART4_RTS	38	OD	Sub TP I2C clock	GPIO_15
I2C_SCL_CAM	95	OD	Camera I2C clock	Can’t use as other I2C and GPIO
I2C_SDA_CAM	94	OD	Camera I2C data	

Note:

When I2C has more than one peripheral, please ensure the uniqueness of peripheral I2C address. When mounting peripherals with high real-time requirements, please do not share I2C with other peripherals.

3.10 ADC Interface

The module provides one ADC interfaces and its accuracy is 15 bit.

Table 3-14 ADC Pin Definition

Pin Name	Pin No.	I/O	Description	Note
ADC	34	AI	ADC detection pin	0~1.7V or 0.3~VBAT Configurable

3.11 LCD Interface

The module video output can support dual-screen display; its screen interface is based on the MIPI_DSI standard and each screen supports 4 sets of high-speed differential data transmission. Each set has a maximum speed of 2.1Gbps and maximally supports 1080P.

Table 3-15 LCD Pin Definition

Pin Name	Pin No.	I/O	Description	Note
VDD_1V8_L6	10	PO	LCD IO voltage	-
VDD_2V85_L17	5	PO	LCD analog power VDD	-
MIPI_LCD0_CLK_P	135	AO	LCD0 MIPI differential clock signal	-
MIPI_LCD0_CLK_M	136	AO		-
MIPI_LCD0_D0_P	137	AI/AO	LCD0 MIPI differential data signal	-
MIPI_LCD0_D0_M	138	AI/AO		-
MIPI_LCD0_D1_P	139	AI/AO		-
MIPI_LCD0_D1_M	140	AI/AO		-
MIPI_LCD0_D2_P	141	AI/AO		-
MIPI_LCD0_D2_M	142	AI/AO		-
MIPI_LCD0_D3_P	143	AI/AO		-
MIPI_LCD0_D3_M	144	AI/AO		-

Pin Name	Pin No.	I/O	Description	Note
LCD0_RST_N	121	DO	LCD0 reset signal	-
MIPI_LCD1_CLK_P	124	AO	LCD1 MIPI differential clock signal	-
MIPI_LCD1_CLK_M	125	AO		-
MIPI_LCD1_D0_P	126	AI/AO	LCD1 MIPI differential data signal	-
MIPI_LCD1_D0_M	127	AI/AO		-
MIPI_LCD1_D1_P	128	AI/AO		-
MIPI_LCD1_D1_M	129	AI/AO		-
MIPI_LCD1_D2_P	130	AI/AO		-
MIPI_LCD1_D2_M	131	AI/AO		-
MIPI_LCD1_D3_P	132	AI/AO		-
MIPI_LCD1_D3_M	133	AI/AO		-
LCD1_RST_N	120	DO	LCD1 reset signal, Active low	-
LCD_BL_PWM	33	DO	LCD backlight PWM control signal	-
GPIO_24	53	DI	LCD0 Tearing Effect signal	-
LCD0_BL_EN	122	DO	LCD backlight enable control signal	-

The reference design of LCD interface circuit is as follows:

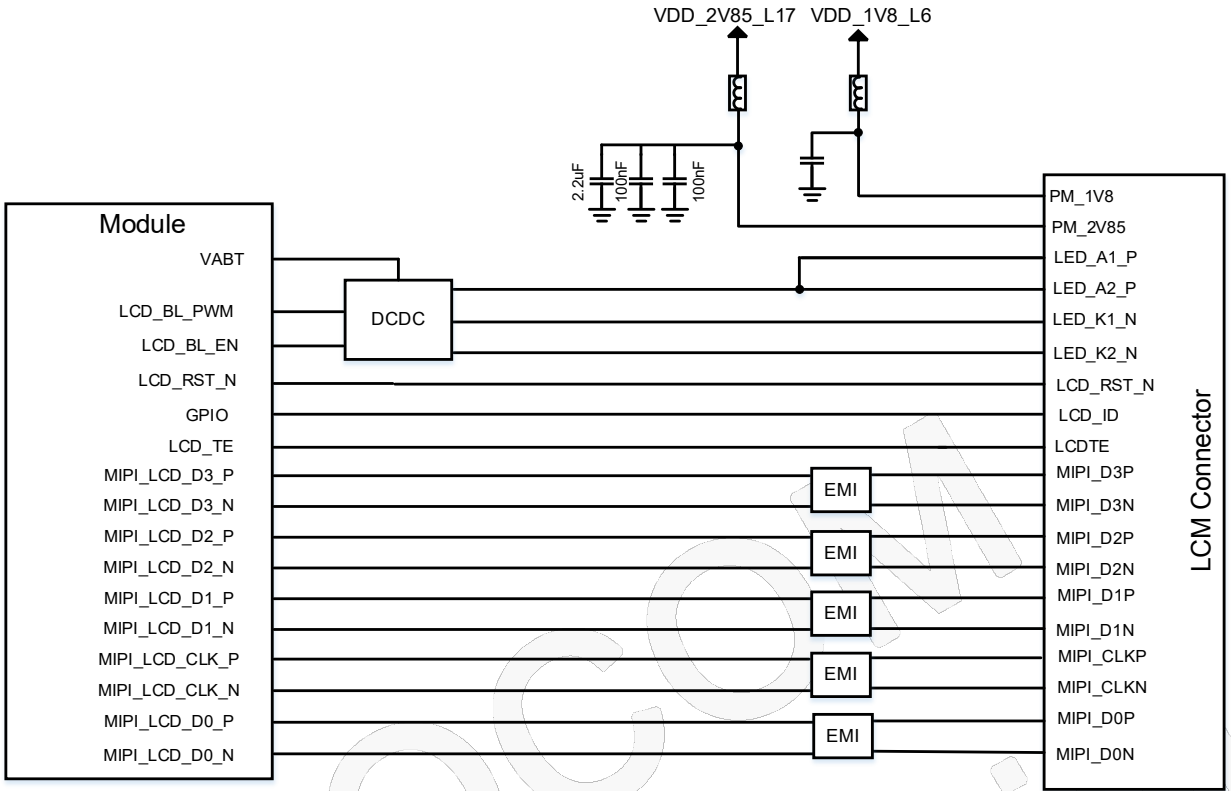

Figure 3-13 Reference Design of LCD Interface Circuit

3.12 Touch Panel Interface

The module provides two sets of I2C interface that can be used to connect the touch panel (TP) and it provides power, interrupt, reset pins. The TP pin definition of the module is shown in the following table:

Table 3-16 TP Pin Definition

Pin Name	Pin No.	I/O	Description	Note
TP_INT_N	119	DI	Main TP interrupt signal	GPIO_65
TP_RST_N	118	DO	Main TP reset signal	GPIO_64
VDD_1V8_L5	12	PO	Main TP IO voltage output	-
VDD_2V8_L10	6	PO	Main TP VDD voltage output	-
I2C_SCL_TP	117	OD	Main TP I2C clock	-
I2C_SDA_TP	167	OD	Main TP I2C data	-
UART4_CTS	39	OD	Secondary TP I2C data	GPIO_14

Pin Name	Pin No.	I/O	Description	Note
UART4_RTS	38	OD	Secondary TP I2C clock	GPIO_15
GPIO_1	46	DO	Secondary TP reset signal	-
GPIO_2	89	DI	Secondary TP interrupt signal	-

The TP reference circuit is as follows:

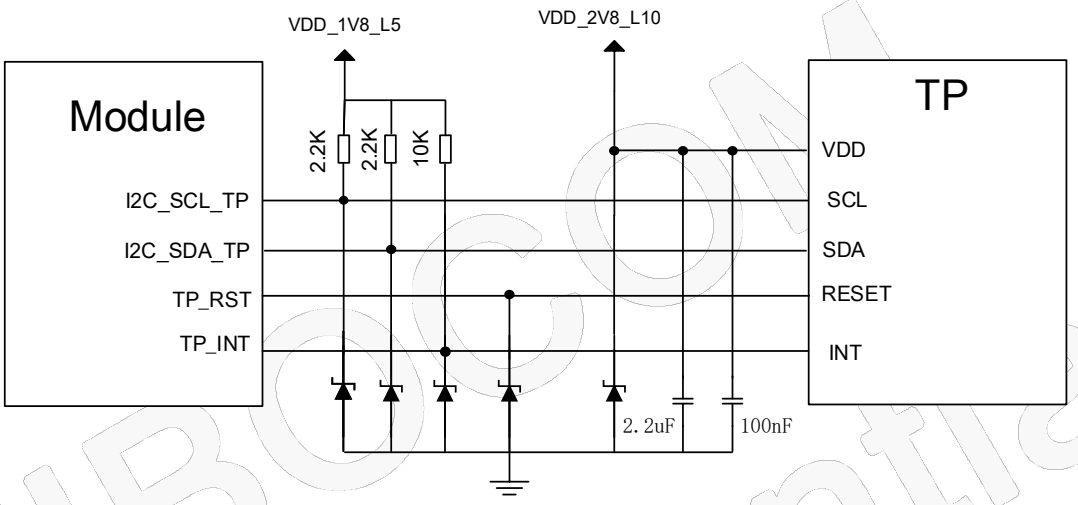

Figure 3-14 Reference Design of TP Interface Circuit

3.13 Camera Interface

The module video input interface is based on the MIPI_CSI standard and supports two cameras.

3.13.1 Main Camera

The main camera uses 4 lane MIPI_CSI differential signal. The pin definition of module main camera is as follows:

Table 3-17 Pin Definition of Main Camera

Pin Name	Pin No.	I/O	Description	Note
VDD_1V8_L6	10	PO	Camera IO voltage	-
VDD_2V8_L22	4	PO	Camera analog voltage	-
VDD_1V1_L2	8	PO	Camera core voltage	-
VDD_2V85_L17	5	PO	Camera focus motor drive voltage	-

Pin Name	Pin No.	I/O	Description	Note
MIPI_CAM0_CLK_P	113	AI	CAM0 MIPI differential clock signal	-
MIPI_CAM0_CLK_M	112	AI		-
MIPI_CAM0_D0_P	111	AI/AO	CAM0 MIPI differential data signal	-
MIPI_CAM0_D0_M	110	AI/AO		-
MIPI_CAM0_D1_P	109	AI/AO		-
MIPI_CAM0_D1_M	108	AI/AO		-
MIPI_CAM0_D2_P	107	AI/AO		-
MIPI_CAM0_D2_M	106	AI/AO		-
MIPI_CAM0_D3_P	105	AI/AO		-
MIPI_CAM0_D3_M	104	AI/AO		-
CAM0_CLK	116	DO	CAM0 master clock signal	-
CAM0_RST_N	92	DO	CAM0 reset signal	-
CAM0_PD_N	93	DO	CAM0 shutdown signal	-
I2C_SCL_CAM	95	OD	I2C clock	-
I2C_SDA_CAM	94	OD	I2C data	-

The reference design of Main camera is as follows:

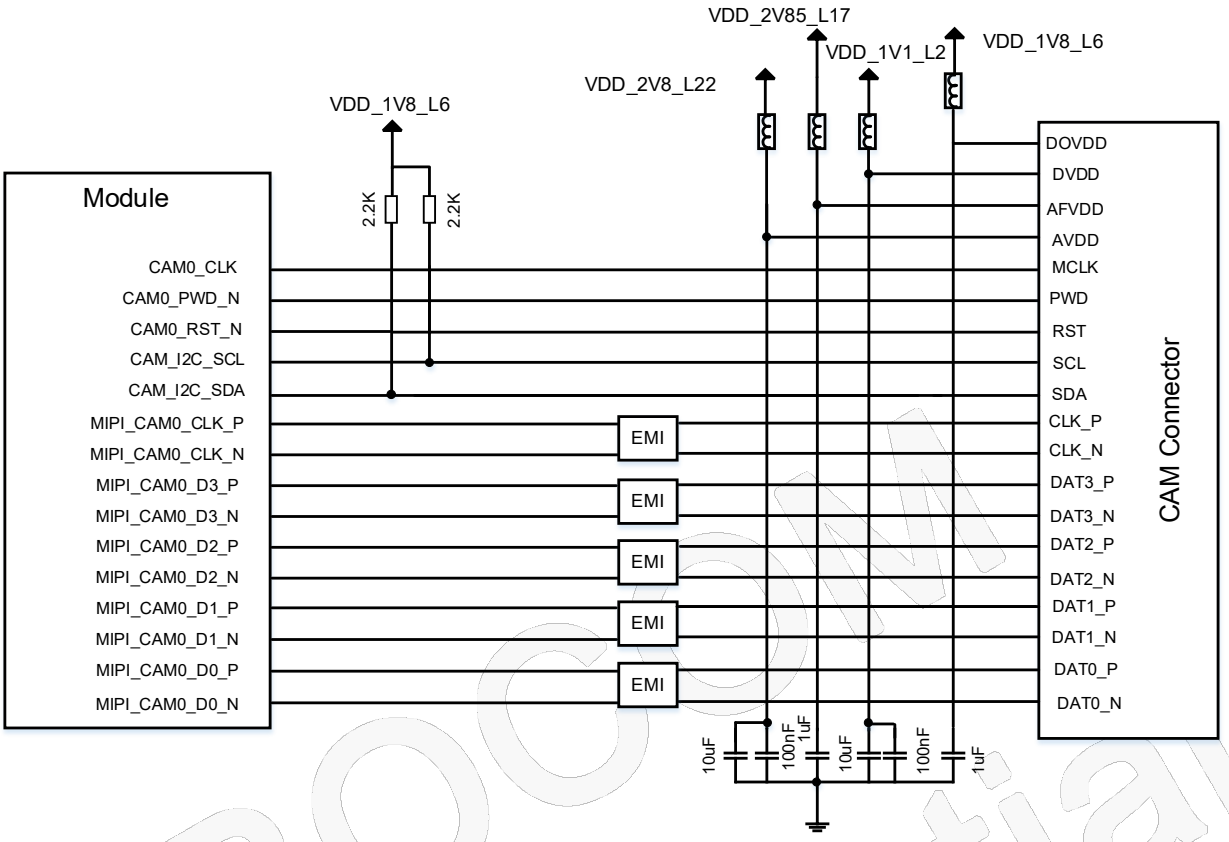

Figure 3-15 Reference Design of Main Camera Circuit

3.13.2 Secondary Camera

The secondary camera uses 2 lane MIPI_CSI differential signal. The pin definition of module secondary camera is as follows:

Table 3-18 Pin Definition of secondary Camera

Pin Name	Pin No.	I/O	Description	Note
VDD_1V8_L6	10	PO	Camera IO voltage	-
VDD_2V8_L22	4	PO	Camera analog voltage	-
VDD_1V175_L23	11	PO	Camera core voltage	-
MIPI_CAM2_CLK_P	102	AI	CAM2 MIPI differential clock signal	-
MIPI_CAM2_CLK_M	101	AI		-
MIPI_CAM2_D0_P	100	AI/AO	CAM2 MIPI differential data signal	-
MIPI_CAM2_D0_M	99	AI/AO		-

Pin Name	Pin No.	I/O	Description	Note
MIPI_CAM2_D1_P	98	AI/AO		-
MIPI_CAM2_D1_M	97	AI/AO		-
CAM2_CLK	115	DO	CAM2 master clock signal	-
CAM2_RST_N	91	DO	CAM2 reset signal	-
CAM2_PD_N	90	DO	CAM2 shutdown signal	-
I2C_SCL_CAM	95	OD	Camera I2C clock signal	-
I2C_SDA_CAM	94	OD	Camera I2C data signal	-

The reference design of secondary camera is as follows:

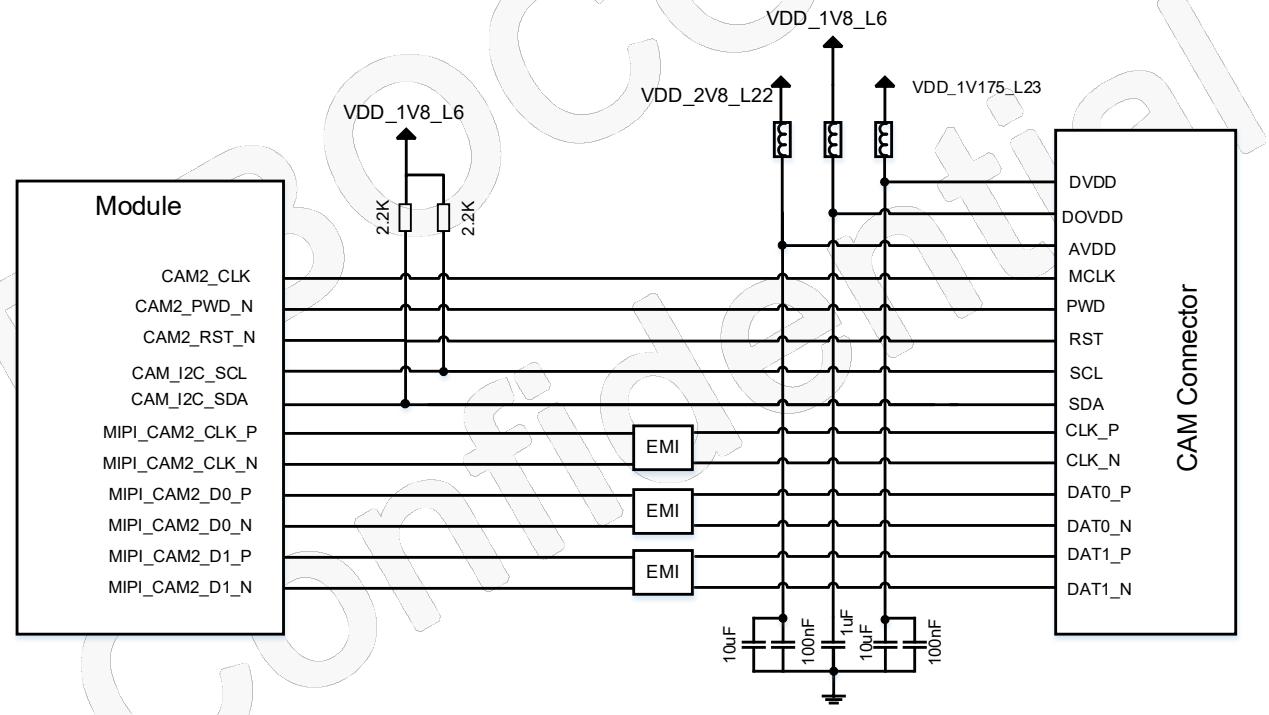

Figure 3-16 Reference Design of secondary Camera Circuit

3.13.3 MIPI Design Considerations

1. MIPI is a high-speed signal. It is recommended to connect the common mode inductor in series near the camera connector to reduce the electromagnetic interference of the circuit.
2. MIPI routing is recommended to be in the inner layer, with three-dimensional grounding;
3. The MIPI signal need to be controlled with a differential impedance of 100Ω and an error of ±10%;

4. The total length of the trace does not exceed 300mm;
5. The intra lane match of mipi signal must be controlled within 0.67mm;
6. The inter lane match of mipi signal must be controlled within 1.3mm;
7. It is recommended that the space of intra lane should be 1.5 times trace width and the differential cable should keep 3 times trace width from other cable;
8. The total component parasitic capacitance on the MIPI differential signal line cannot exceed 1.0pF;

Other design considerations:

1. CAM_CLK is a high-speed clock signal and requires three-dimensional grounding;
2. If the main and secondary cameras share the I2C, you need to confirm that the I2C addresses of the two cameras do not conflict;
3. The analog voltage AVDD routing should be away from interference sources, otherwise it is easy to bring interference of power noise; the AVDD suggest to add LDO with high PSRR ability, place it close to camera.

3.14 Sensor Interface

The module uses I2C to communicate with sensors and supports various types of sensors, including acceleration sensor, distance and ambient light sensor, geomagnetic sensor, gyroscopes, etc.

Table 3-19 Sensor Control Pin Description

Pin Name	Pin No.	I/O	Description	Note
I2C_SCL_EXT	77	OD	I2C clock	-
I2C_SDA_EXT	78	OD	I2C data	-
GPIO_42	56	DI	The configuration is acceleration sensor interrupt input by default	-
GPIO_43	57	DI	Default configuration is ambient light & distance sensor interrupt input	-
GPIO_45	66	DI	Default configuration is gyroscope interrupt input	-

3.15 Audio

3.15.1 Definition of Audio Interface

The module supports analog audio interface, 2-lane input and 4-lane output.

Table 3-20 Definition of Audio Interface

Pin Name	Pin No.	I/O	Description	Note
SPK_P	16	AO	Class D amplifier differential output	-
SPK_M	17	AO		-
REC_P	19	AO	Handset differential output	-
REC_M	20	AO		-
HPH_L	21	AO	Headphone left channel output	-
HPH_GND	22	/	Headphone grounding	-
HPH_R	23	AO	Headphone right channel output	-
HPH_DET	24	AI	Headphone plug detection	-
MIC2_P	28	AI	Headphone MIC input	-
MIC1_M	30	AI	Main MIC differential input-	-
MIC1_P	31	AI	Main MIC differential input +	-
LINEOUT_P	202	AO	Audio lineout differential output	-
LINEOUT_M	203	AO		-

Note:

1) The MIC bias circuit has been added to the module, and no external addition is required;

2) The SPK is configured class D amplifier and cannot be connected to an external amplifier. It is recommended to connect 8Ω speakers. Note that the route width must meet the power rating requirements. If an external audio amplifier is required, the input can choose headphone left and right channels (single-ended input) or lineout (differential input);

3) The reference ground of the headphone has already grounded in the module. The external circuit is recommended not to be grounded and resistor can be reserved;

4) It is recommended to connect 32Ω handset;

5) Reduce noise and improve audio quality, the following approaches are recommended:

- Keep audio PCB routing away from the antenna and high-frequency digital signal
- Reserve LC filter circuit in audio circuit to reduce EMI
- Audio routing needs to be masked

3.15.2 Microphone Circuit Design

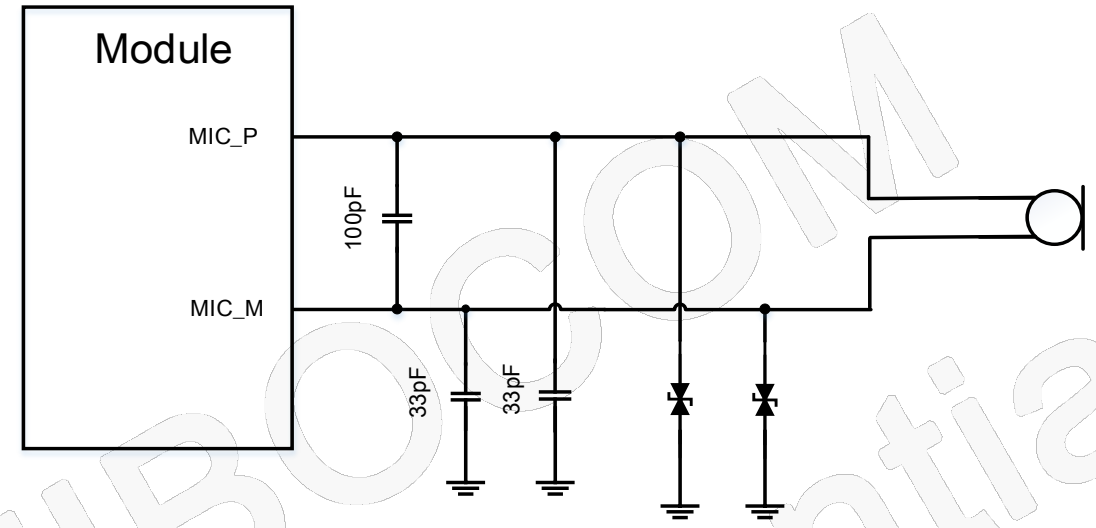

Figure 3-17 Reference Design of Microphone Circuit

3.15.3 Handset Circuit Design

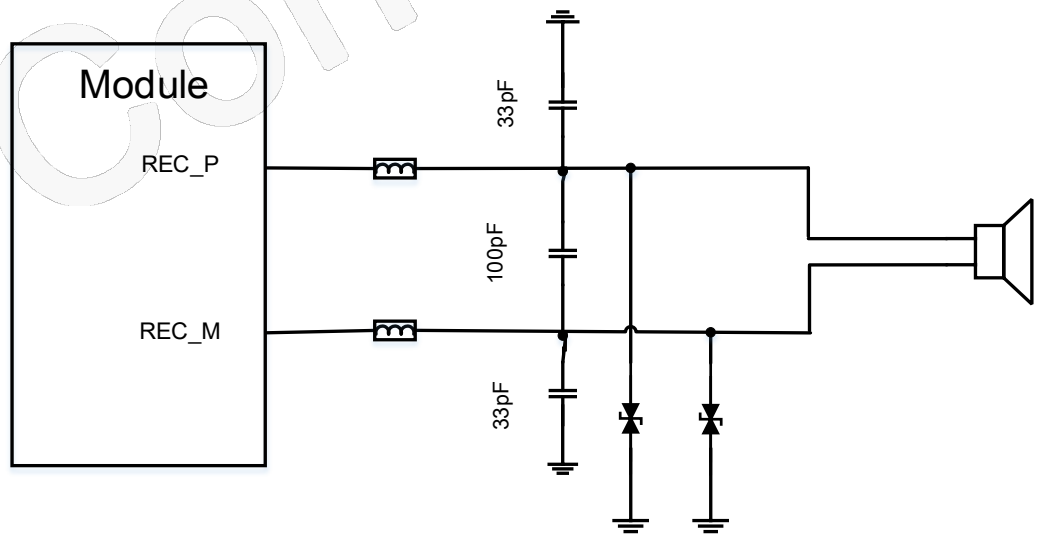

Figure 3-18 Reference Design of Handset Circuit

3.15.4 Headphone Interface Circuit Design

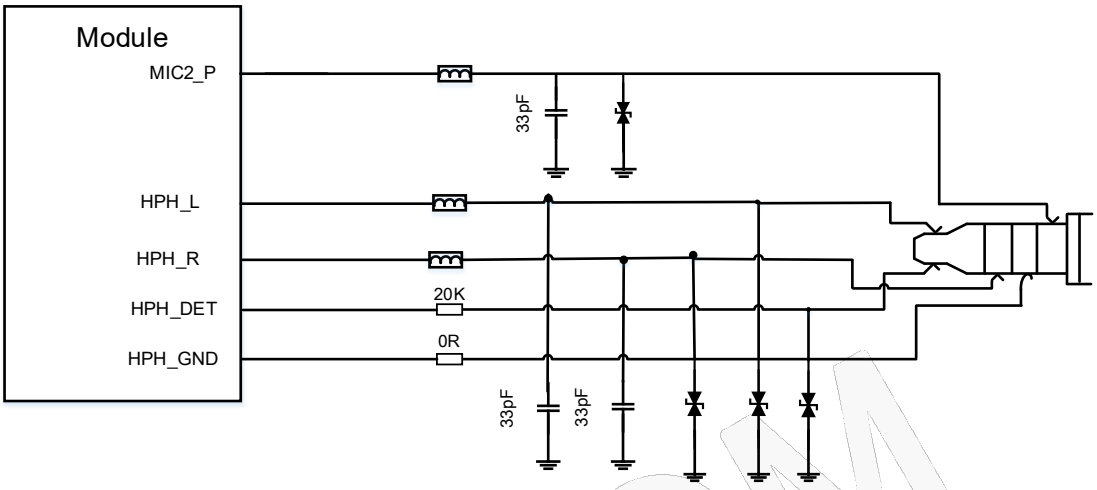

Figure 3-19 Reference Design of Headphone Circuit

Note：

Recommendation TVS for headphone to prevent system level issue, please choose bidirectional device.

3.15.5 Speaker Circuit Design

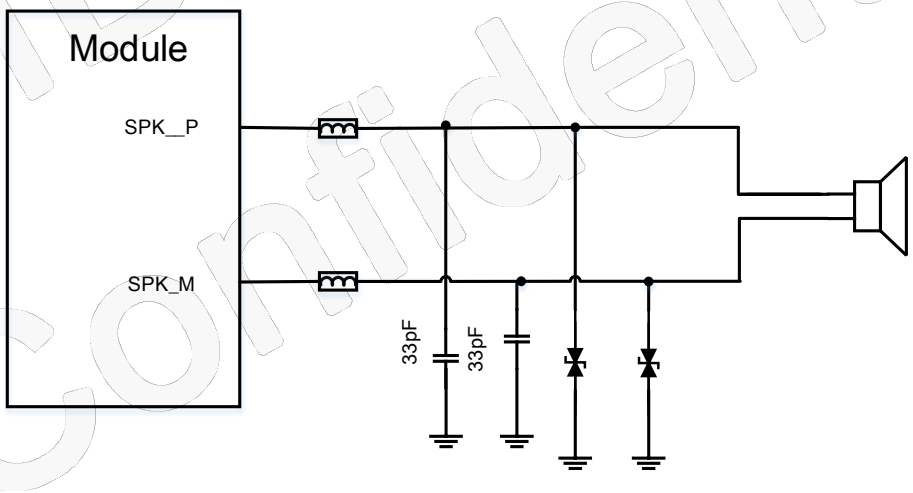

Figure 3-20 Reference Design of Speaker Circuit

3.15.6 LINEOUT Circuit Design

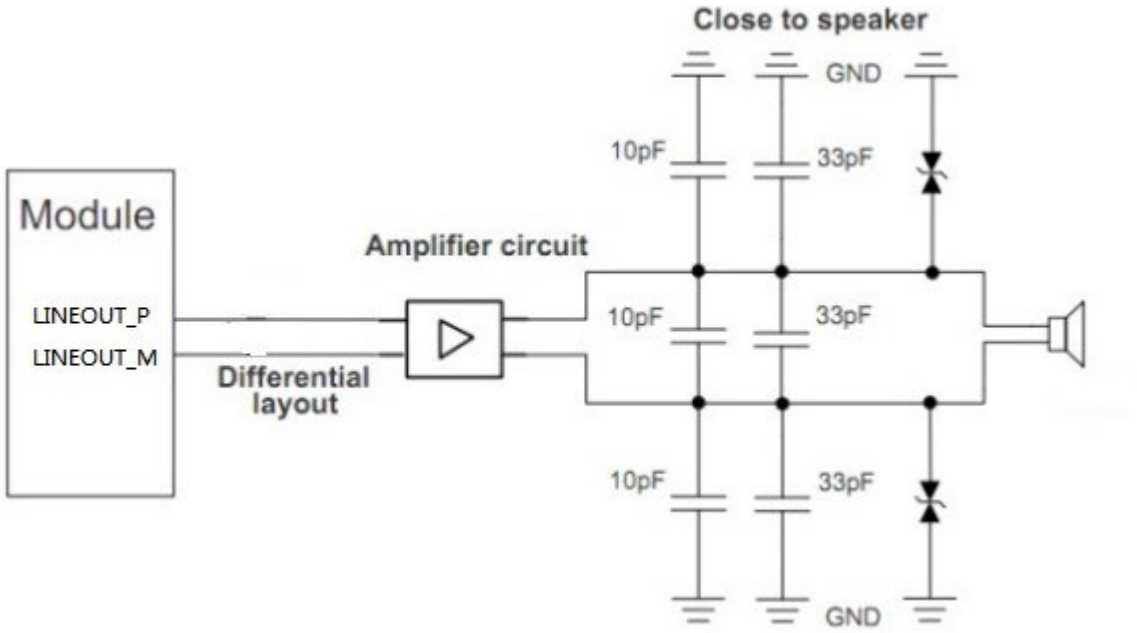

Figure 3-21 Reference Design of LINEOUT Circuit

3.16 Forced Download Interface Design

The module provides the FORCE_BOOT pin as an emergency download interface. Connect the FORCE_BOOT and VDD_1V8_L5 pin in a short circuit when power on, the module can enter the emergency download mode which is used for the final processing mode when the product fails to power on or run normally. To facilitate the subsequent software upgrade and product debugging, please reserve this pin.

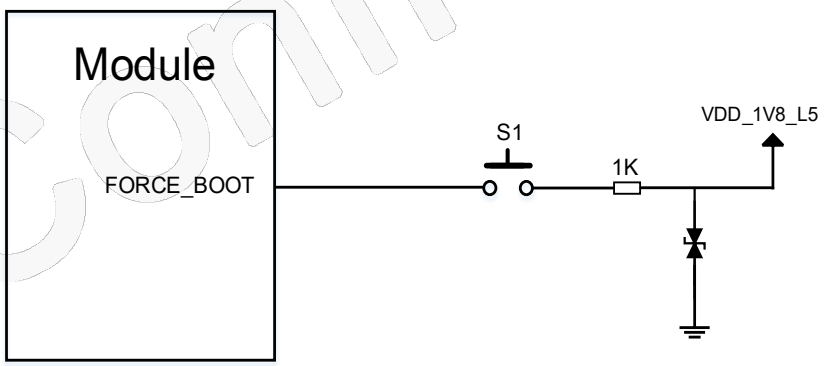

Figure 3-22 Reference Design of FORCE_BOOT Circuit

4 Antenna Interface

The module supports 2/3/4G main antenna/diversity reception antenna, WIFI/BT antenna and GNSS antenna.

4.1 MAIN/DRX Antenna

The module provides two 2G/3G/4G antenna interfaces. The ANT_MAIN is used to receive and transmit RF signal, the ANT_DRX is used for diversity reception.

Table 4-1 MAIN/DRX Antenna Interface Definition

Pin Name	Pin No.	I/O	Description	Note
ANT_MAIN	60	I/O	2G/3G/4G antenna interface	-
ANT_DRX	41	AI	Diversity reception antenna	-

4.1.1 Operating Band

Table 4-2 Module Operating Band

Mode	Band	Tx (MHz)	Rx (MHz)
GSM	900	880 - 915	925 - 960
	1800	1710 - 1785	1805 - 1880
WCDMA	Band 1	1920 - 1980	2110 - 2170
	Band 8	880 - 915	925 - 960
CDMA	Band 5	824 - 849	869 - 894
TDSCDMA	Band 34	2010 - 2025	2010 - 2025
	Band 39	1880 - 1920	1880 - 1920
LTE FDD	Band 1	1920 - 1980	2110 - 2170
	Band 3	1710 - 1785	1805 - 1880
	Band 5	824 - 849	869 - 894

Mode	Band	Tx (MHz)	Rx (MHz)
	Band 8	880 - 915	925 - 960
LTE TDD	Band 34	2010 - 2025	2010 - 2025
	Band 38	2570 - 2620	2570 - 2620
	Band 39	1880 - 1920	1880 - 1920
	Band 40	2300 - 2400	2300 - 2400
	Band 41	2555 - 2655	2555 - 2655

4.1.2 Circuit Reference Design

For use of the module, it is necessary to connect the antenna pin with the RF connector or antenna feed point on the main board via an RF trace. Microstrip trace is recommended for RF trace, with insertion loss within 0.2dB and impedance at 50Ω.

A π-type circuit is reserved between the module and the antenna connector (or feed point) for antenna debugging. Two parallel component are directly connected across the RF trace and should not pull out a branch, as the figure shows:

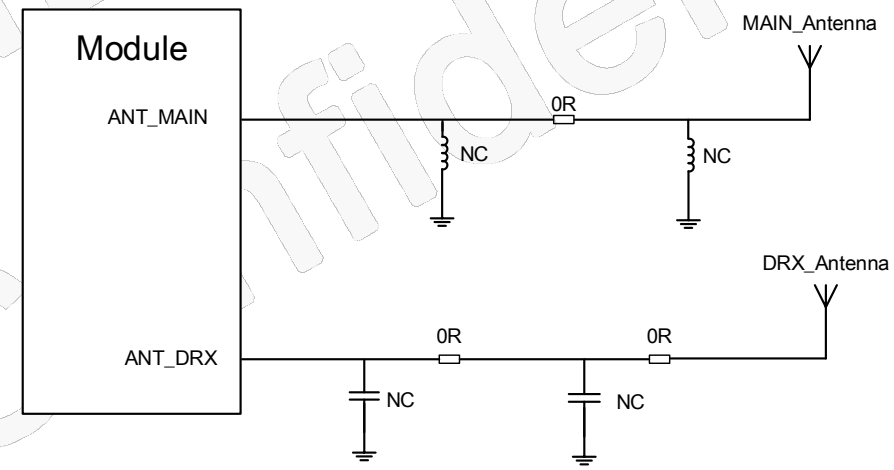

Figure 4-1 MAIN/DRX Antenna Connection

4.2 WIFI/BT Antenna

Microstrip trace is recommended for the WIFI/BT RF route, with insertion loss within 0.2dB and impedance at 50Ω.

Table 4-3 WIFI/BT Antenna Interface Definition

Pin Name	Pin No.	I/O	Description	Note
ANT_BT/WIFI	2	I/O	WIFI/BT antenna interface	-

4.2.1 Operating Frequency

Table 4-4 WIFI/BT Operating Frequency

Mode	Frequency	unit
WIFI	2402-2482	MHz
	5180-5825	MHz
BT4.2	2402-2480	MHz

4.2.2 Circuit Reference Design

WIFI/BT antenna connection reference circuit is shown as follows

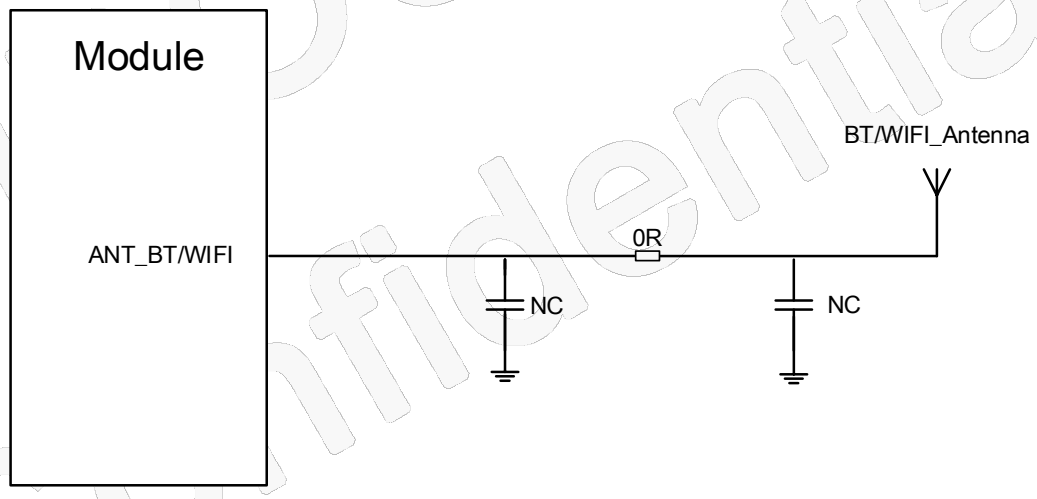

Figure 4-2 WIFI/BT Antenna Connection

4.3 GNSS Antenna

GNSS supports GPS/GLONASS/BeiDou.

Table 4-5 GNSS Antenna Interface Definition

Pin Name	Pin No.	I/O	Description	Note
ANT_GNSS	49	AI	GNSS antenna interface	-

4.3.1 Operating Frequency

Table 4-6 GNSS Operating Frequency

Mode	Frequency	unit
GPS	1575.42±1.023	MHz
GLONASS	1597.42-1605.8	MHz
BeiDou	1561.098±2.046	MHz

4.3.2 Circuit Reference Design

Passive antenna reference design：

The module has a built-in LNA. The passive antenna is used in the design of the device. Microstrip trace is recommended for the GNSS RF route, with insertion loss within 0.2dB and impedance at 50Ω. The connection reference circuit is shown as follows:

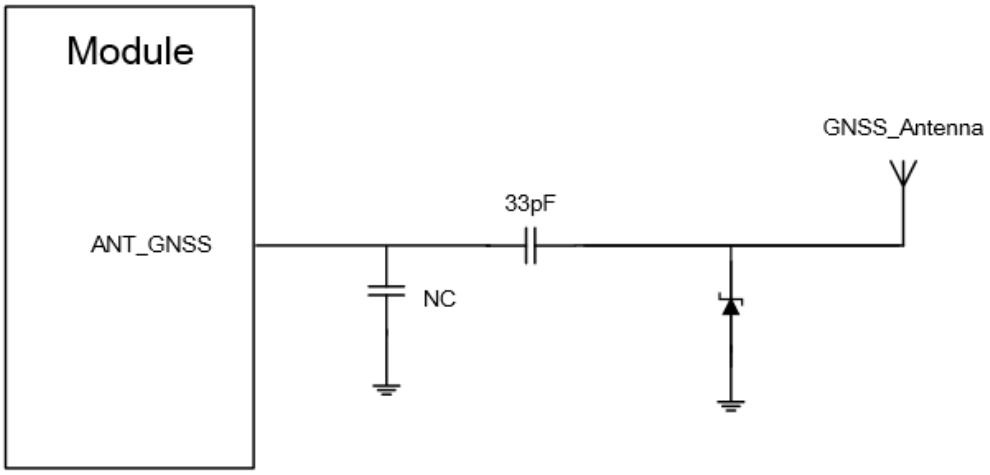

Figure 4-3 GNSS passive Antenna Connection

Note：

Adding TVS tube can improve ESD performance of GNSS. The recommended TVS tube features are as follows: CJ: 0.5pF, ESD clamping voltage: 5.0V, Recommended unit: ESD9D5U.

Active antenna reference design：

The power supply of the active antenna is fed from the signal line of the antenna through the inductance of 56nH. The common active antenna provides power for 3.3V ~ 5.0V.

Active antenna itself power consumption is very small, but the power supply is required to be stable and

clean. It is recommended to use LDO with high performance to supply power to the antenna.

If active antenna Built-in LNA gain > 17dB , we need use the reserved π matching to increase the attenuation network。

The connection reference circuit is shown as follows:

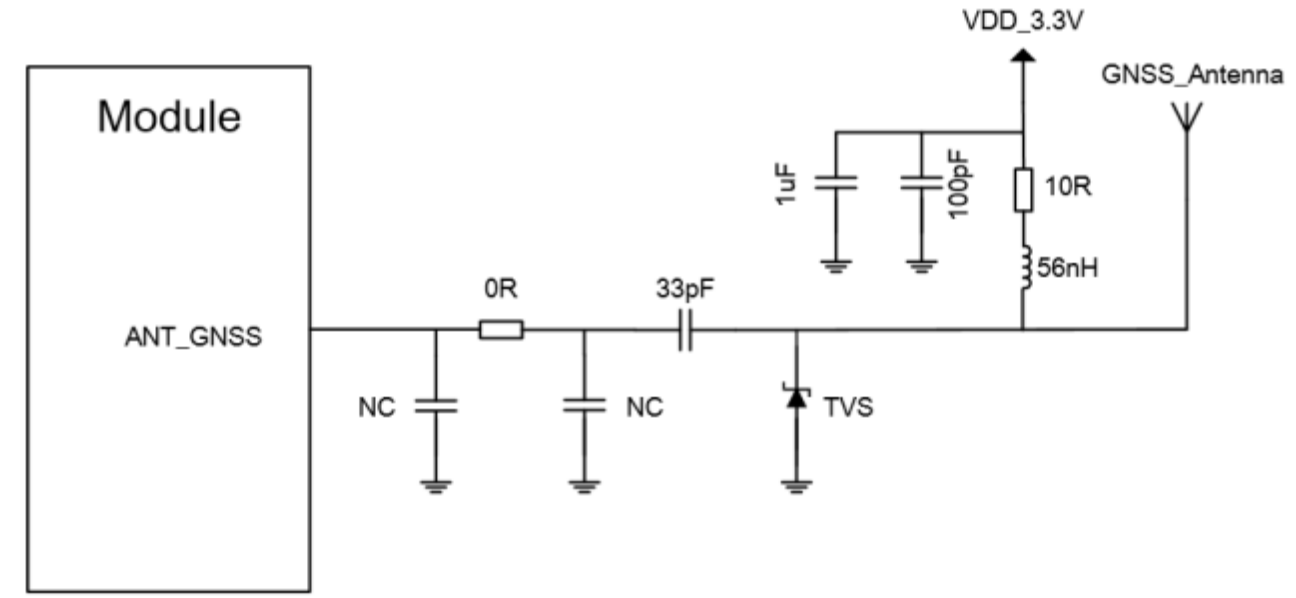

Figure 4-4 GNSS active Antenna Connection

4.4 Antenna Requirement

The module provides four antenna interfaces: main, diversity, WIFI/BT and GNSS. The antenna requirements are as follows:

Table 4-7 Module Antenna Requirements

Module Antenna Requirements	
Standard	**Antenna requirements**
GSM/WCDMA/CDMA/TDSCDMA/LTE	VSWR: ≤ 2 Gain (dBi): 1 Max input power (W): 5 Input impedance (Ω): 50 Polarization type: vertical direction Insertion loss: < 1dB (0.7-1GHz) Insertion loss: < 1.5dB(1.4-2.2GHz) Insertion loss: < 2dB (2.3-2.7GHz)

Module Antenna Requirements	
Standard	**Antenna requirements**
WIFI/BT	VSWR: ≤ 2 Gain (dBi): 1 Max input power (W): 5 Input impedance (Ω): 50 Polarization type: vertical direction Insertion loss: < 1dB
GNSS	Frequency range: 1559MHz~1607MHz Polarization type: right-circular or linear polarization VSWR: < 2 (typical) Passive antenna gain: > 0dBi Active antenna NF: < 15dB (typical) Active antenna gain: > -2dBi Active antenna Built-in LNA gain : < 17dB (typical)

5 RF PCB Layout Design Guide

For user PCB, the characteristic impedance of all RF signal traces should be within 50Ω. In general, the impedance of the RF signal trace is determined by the dielectric constant of the material, the trace width (W), the ground clearance (S) and the height of the reference ground plane (H). The control of the characteristic impedance of the PCB usually in two ways: microstrip trace and coplanar waveguide. To illustrate the design principles, the following figures show the structural designs of microstrip trace and coplanar waveguide when the impedance cable is at 50Ω.

- Microstrip trace entirety structure

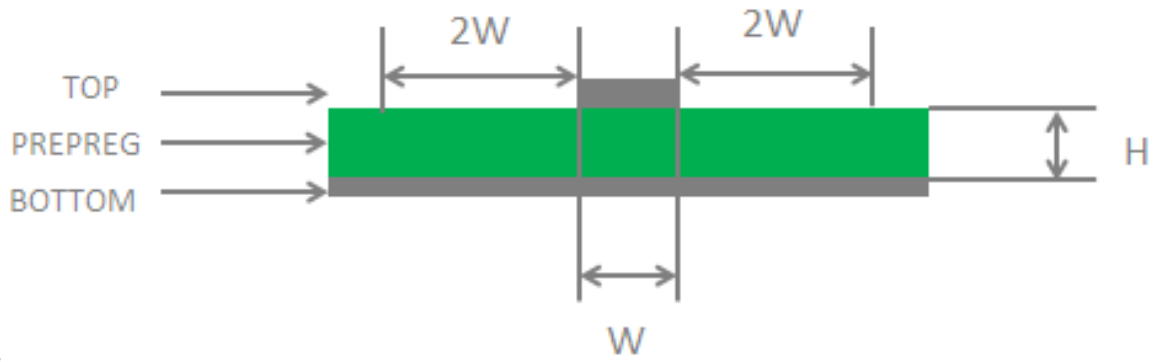

Figure 5-1 Two-layer PCB Microstrip Cable Structure

- Coplanar waveguide entirety structure

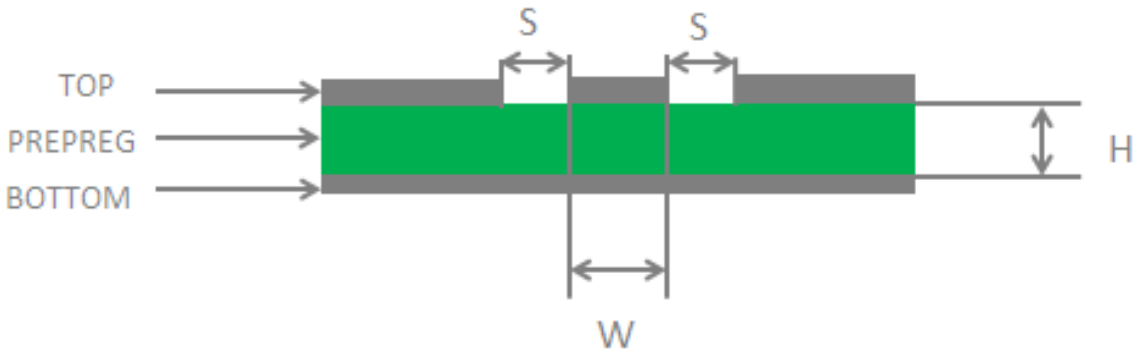

Figure 5-2 Two-layer PCB Coplanar Waveguide Structure

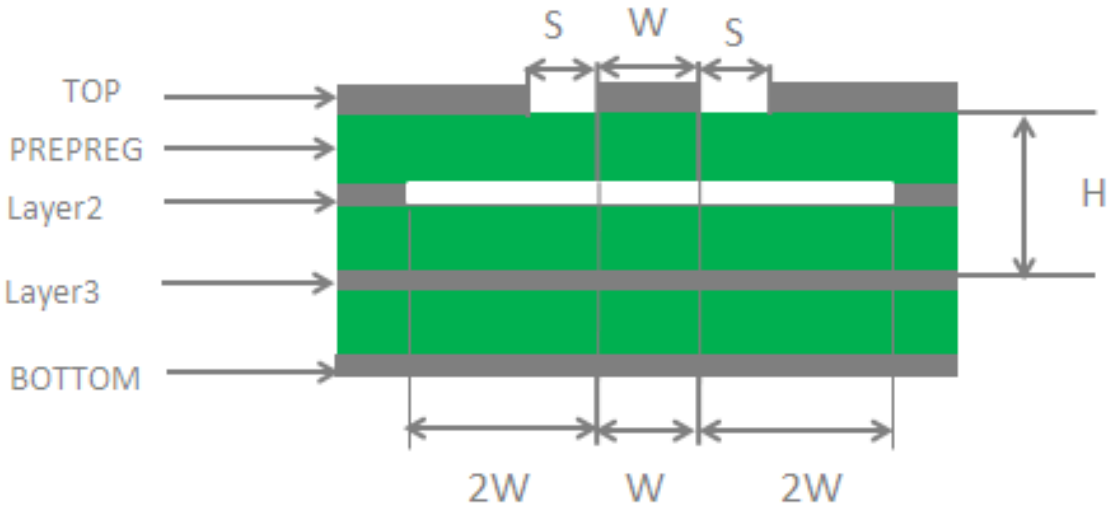

Figure 5-3 Four-layer PCB Coplanar Waveguide Structure (Reference Ground layer3)

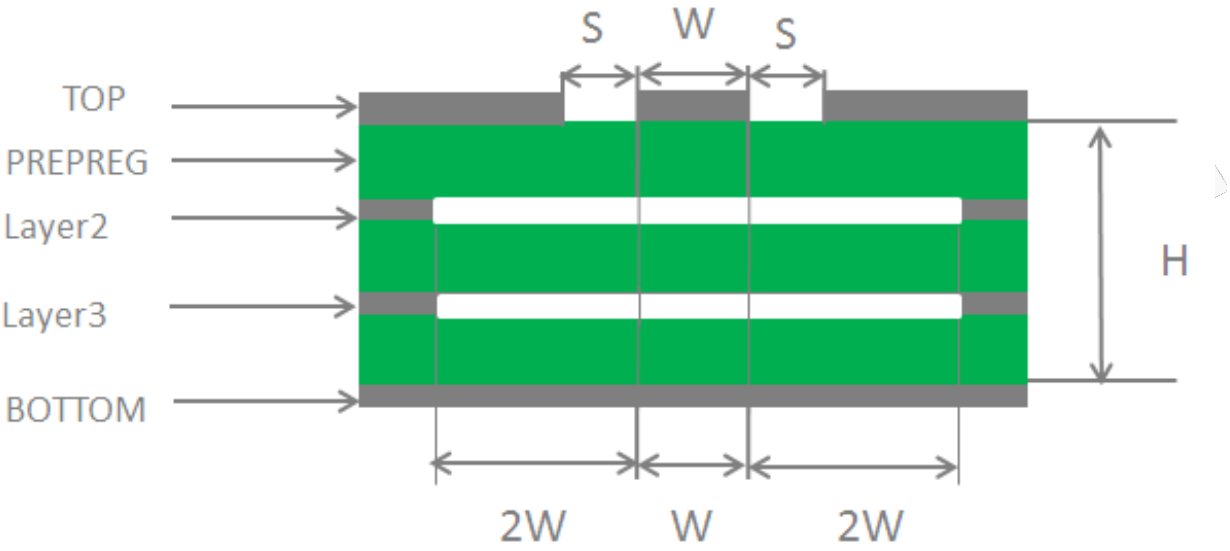

Figure 5-4 Four-layer PCB Coplanar Waveguide Structure (Reference Ground layer4)

In the design of RF antenna interface circuit, in order to ensure good performance and reliability of the RF signal, it is recommended to observe the following principles:

- The impedance simulation tool should be used to accurately control the RF signal cable at 50Ω impedance.
- The GND pin adjacent to the RF pin should not have thermal welding plate and should be in full contact with the ground.
- The distance between the RF pin and the RF connector should be as short as possible. At the same time, avoid the right-angle route. The recommended route angle is 135 degree.
- Attention should be paid to the establishment of the component package and the signal pin should be kept at a certain distance from the ground.
- The reference ground plane of the RF signal trace should be entirety; adding a certain amount of

ground holes around the signal and the reference ground can help improve the RF performance; the distance between the ground hole and the signal trace should be at least 2 times the trace width (2*W).

6 WIFI and Bluetooth

6.1 WIFI Overview

The module supports 2.4G and 5G WLAN wireless communications and 802.11a, 802.11b, 802.11g, 802.11n, 802.11ac standards, with a maximum speed up to 433 Mbps. Its characteristics are as follows:

- Support Wake-on-WLAN (WoWLAN)
- Support ad hoc mode
- Support WAPI
- Support AP mode
- Support Wi-Fi Direct
- Support MCS 0-7 for HT20 and HT40
- Support MCS 0-8 for VHT20
- Support MCS 0-9 for VHT40 and VHT80

6.2 WIFI Performance Index

Test condition: VBAT: 3.8V, temperature: 25° C.

Table 6-1 WIFI Transmit Power

Frequency	Mode	Date Rate	Bandwidth (MHz)	TX Power (dBm)
2.4G	802.11b	1Mbps	20	17.0±3
		11Mbps	20	17.0±3
	802.11g	6Mbps	20	16.0±3
		54Mbps	20	14.0±3
	802.11n	MCS0	20	15.0±3
		MCS7	20	13.0±3
		MCS0	40	15.0±3
		MCS7	40	12.0±3
5G	802.11a	6Mbps	20	18.0±3

Frequency	Mode	Date Rate	Bandwidth (MHz)	TX Power (dBm)
		54Mbps	20	16.0±3
	802.11n	MCS0	20	17.0±3
		MCS7	20	14.0±3
	802.11n	MCS0	40	17.0±3
		MCS7	40	14.0±3
	802.11ac	MCS0	20	17.0±3
		MCS8	20	14.0±3
		MCS0	40	17.0±3
		MCS9	40	13.0±3
		MCS0	80	17.0±3
		MCS9	80	13.0±3

Table 6-2 WIFI Reception Sensitivity

Frequency	Mode	Date Rate	Bandwidth (MHz)	Sensitivity (dBm)
2.4G	802.11b	1Mbps	20	-91.0
		11Mbps	20	-89.0
	802.11g	6Mbps	20	-91.0
		54Mbps	20	-73.0
	802.11n	MCS0	20	-90.0
		MCS7	20	-71.0
	802.11n	MCS0	40	-87.0
		MCS7	40	-67.0
5G	802.11a	6Mbps	20	-90.0

Frequency	Mode	Date Rate	Bandwidth (MHz)	Sensitivity (dBm)
		54Mbps	20	-73.0
	802.11n	MCS0	20	-89.0
		MCS7	20	-71.0
	802.11n	MCS0	40	-87
		MCS7	40	-68
	802.11ac	MCS0	20	-89
		MCS8	20	-66
		MCS0	40	-88
		MCS9	40	-61
		MCS0	80	-81
		MCS9	80	-54

6.3 Bluetooth Overview

The module supports BT4.2 (BR/EDR+BLE) standards. The modulation method supports GFSK, 8-DPSK and π/4-DQPSK.BR/EDR. Channel bandwidth is 1MHz and can accommodate 79 channels. The BLE channel bandwidth is 2MHz and can accommodate 40 channels. Its main features are as follows:

- BT 4.2 + BR/EDR + BLE
- Support for ANT protocol
- Support for BT-WLAN coexistence operation, including optional concurrent receive
- Up to 3.5 piconets (master, slave and page scanning)

Table 6-3 BT Rate and Version Information

Version	Date Rate	Throughput	Note
BT1.2	1Mbit/s	> 80Kbit/s	-
BT2.0+EDR	2Mbit/s	> 80Kbit/s	--
BT3.0+HS	24Mbit/s	Refer 3.0+HS	-

BT4.2 LE	24Mbit/s	Refer 4.0 LE	-

6.4 Bluetooth Performance Index

Test condition: VBAT: 3.8V, temperature: 25° C.

Table 6-4 BT Performance Index

Type	DH-5	2-DH5	3-DH5	Unit
Transmitter	9±2.5	7±2.5	6.5±2.5	dBm
Sensitivity[2)]	-89	-87	-85	dBm

Note:

Here the sensitivity is typical.

7 GNSS

7.1 Overview

The module supports multiple positioning systems including GPS, GLONASS and Beidou. The module is embedded in LNA which can effectively improve the sensitivity of GNSS.

7.2 Performance Index

Test condition: VBAT: 3.8V, temperature: 25°C.

Table 7-1 GNSS Positioning Performance

Parameter	Description	Typical Result	Unit
Sensitivity	Acquisition	-146	dBm
	Tracking	-158	dBm
C/No	-130dBm	40	dB-Hz
TTFF	Cold Start	35	s
	Warm Start	30	s
	Hot Start	2	s
CEP	Static accuracy	3	m

8 Electrical, Reliability and RF Performance

8.1 Recommended Parameters

Table 8-1 Recommended Parameters

Parameter	Min	Nominal	Max	Unit
VBAT	3.5	3.8	4.35	V
USB_VBUS	4.75	5	5.25	V
VRTC	2.0	3.0	3.25	V
Operating Temperature	-30	25	75	℃
Storage Temperature	-40	25	85	℃

8.2 Operating Current

Test condition: VBAT: 3.8V, temperature: 25°C. When testing GSM's sleep current with the test white card, change NV947 to 0, but not the real.

Table 8-2 Operating Current

Parameter	Description	Condition	Typical Result	Unit
I_{off}	Power Off	Power Off	25	uA
I_{sleep}	GSM	MFRMS=5	4.2	mA
	CDMA	Slot Cycle Index=2	4.4	
	WCDMA	DRX=8	4	
	TD-SCDMA	DRX=8	4.4	
	TDD LTE	DPC(Default Paging Cycle)=#256	4.4	
	FDD LTE	DPC(Default Paging Cycle)=#256	4.4	

Parameter	Description	Condition	Typical Result	Unit
	Radio Off	AT+CFUN=4 Flight Mode	3	
$I_{GSM-RMS}$	GSM voice RMS Current	EGSM900@ PCL=5	270	mA
		EGSM900@ PCL=19	100	
		DCS1800@ PCL=0	240	
		DCS1800@ PCL=15	120	
$I_{GSM-MAX}$	GSM voice Peak current	EGSM900@ PCL=5	2460	mA
		DCS1800@ PCL=0	1580	
$I_{GPRS-RMS}$	GPRS data RMS Current	EGSM900@Gamma=3(1UL/4DL)	260	mA
		EGSM900@Gamma=3(4UL/1DL)	610	
		DCS1800@Gamma=3(1UL/4DL)	230	
		DCS1800@Gamma=3(4UL/1DL)	630	
$I_{EGPRS-RMS}$	EGPRS data RMS Current	EGSM900@Gamma=6(1UL/4DL)	200	mA
		EGSM900@Gamma=6(4UL/1DL)	440	
		DCS1800@Gamma=5(1UL/4DL)	200	
		DCS1800@Gamma=5(4UL/1DL)	460	
$I_{CDMA-RMS}$	CDMA RMS Current	BC0@ max power	600	mA
$I_{TDSCDMA-RMS}$	TDSCDMA RMS Current	Band34@ max power	200	mA
		Band39@ max power	200	
$I_{WCDMA-RMS}$	WCDMA RMS Current	Band1@ max power	600	mA
		Band8@ max power	550	
$I_{LTE-RMS}$	FDD data RMS Current	Band1@max power(10MHz,1RB)	650	mA
		Band3@max power(10MHz,1RB)	650	

Parameter	Description	Condition	Typical Result	Unit
		Band5@max power(10MHz,1RB)	580	
		Band8@max power(10MHz,1RB)	550	
	TDD data RMS Current	Band34@max power(10MHz,1RB)	350	
		Band38@max power(10MHz,1RB)	400	
		Band39@max power(10MHz,1RB)	370	
		Band40@max power(10MHz,1RB)	370	
		Band41@max power(10MHz,1RB)	400	

8.3 RF Transmit Power

The transmit power of each band of the module is shown in the following table:

Test condition: VBAT: 3.8V, temperature: 25°C, LTE max power@10MHz 12RB.

Table 8-3 Module RF Transmit Power

Mode	Band	Max Power (dBm)	Min Power (dBm)
GSM	900(GMSK)	33±2	5±5
	1800(GMSK)	30±2	0±5
GSM	900(8PSK)	27.0±3	5±5
	1800(8PSK)	25.0±3	0±5
EVDO/CDMA	BC0	24.0+3/-1	< -49
WCDMA	Band 1	24+1/-3	< -49
	Band 8	24+1/-3	< -49
TD-SCDMA	Band 34	24+1/-3	< -49

Mode	Band	Max Power (dBm)	Min Power (dBm)
	Band 39	24+1/-3	< -49
LTE FDD	Band 1	23.0±2	< -39
	Band 3	23.0±2	< -39
	Band 5	23.0±2	< -39
	Band 8	23.0±2	< -39
LTE TDD	Band 34	23.0±2	< -39
	Band 38	23.0±2	< -39
	Band 39	23.0±2	< -39
	Band 40	23.0±2	< -39
	Band 41	23.0±2	< -39

8.4 RF Receiver Sensitivity

The sensitivity of each frequency band of the module is shown in the following table, the following test results are typical values.

The SC820-CN-20 only supports LTE diversity.

Test condition: VBAT: 3.8V, temperature: 25°C, LTE sensitivity@10MHz,RB configuration refer to 3GPP.

Table 8-4 Module RF Receiver Sensitivity

Mode	Band	Primary	Diversity	PRX + Div	3GPP Requirement	Unit
GSM	900	-109.5	-108	-111	-102.0	dBm
	1800	-107.5	-108.5	-110	-102.0	dBm
CDMA	BC0	-108	NA	NA	-104.0	dBm
WCDMA	Band 1	-109	-110	-112	-106.7	dBm
	Band 8	-110	-110.5	-113	-103.7	dBm

Mode	Band	Primary	Diversity	PRX + Div	3GPP Requirement	Unit
TD-SCDMA	Band 34	-110	-110	-112	-108.0	dBm
	Band 39	-110	-110	-112	-108.0	dBm
LTE FDD	Band 1	-97	-99	-102	-96.3	dBm
	Band 3	-97	-98	-101	-93.3	dBm
	Band 5	-98	-98	-101	-93.3	dBm
	Band 8	-98	-98	-101	-93.3	dBm
LTE TDD	Band 34	-97	-98	-100	-96.3	dBm
	Band 38	-96	-96.5	-100	-96.3	dBm
	Band 39	-98	-98	-101	-96.3	dBm
	Band 40	-97	-98	-100	-96.3	dBm
	Band 41	-96	-96.5	-100	-94.3	dBm

8.5 Electrostatic Protection

In the application of the module, due to static electricity generated by human body and charged friction between micro-electronics, etc. discharging to the module through various channels that may cause damage, so ESD protection should be taken seriously attention. In the process of R&D, production assembly and testing, especially in product design, ESD protection measures should be taken. For example, anti-static protection should be added at the designed circuit interface and the points susceptible to electrostatic discharge or impact. Anti-static gloves should be worn during production. ESD performance parameters table 1-6 (Temperature: 25°C, Humidity: 45 %~60%).

Table 8-5 ESD Performance

Test Point	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	KV
Antenna interface	±4	±8	KV
Other interface	±0.5	±1	KV

9 Structural Specification

9.1 Product Appearance

The module appearance is shown in the figure ,product appearance depends on goods.

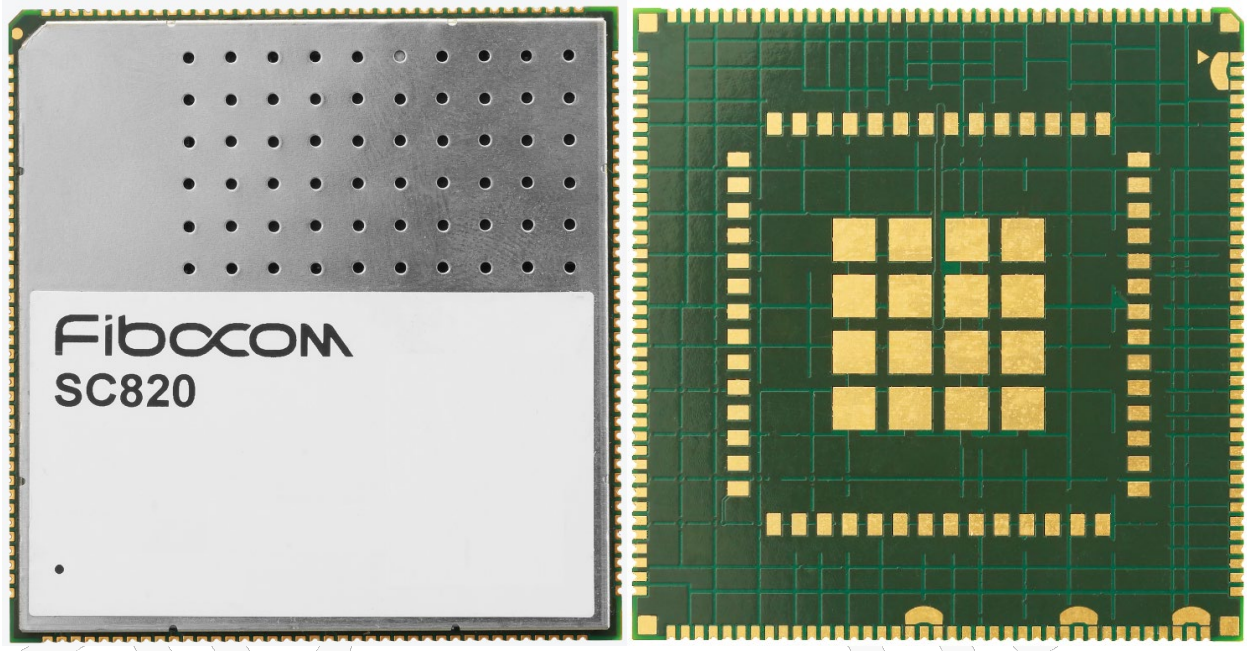

Figure 9-1 Module Product Appearance

9.2 Structural Dimension

The structural dimension of the module is shown in the figure:

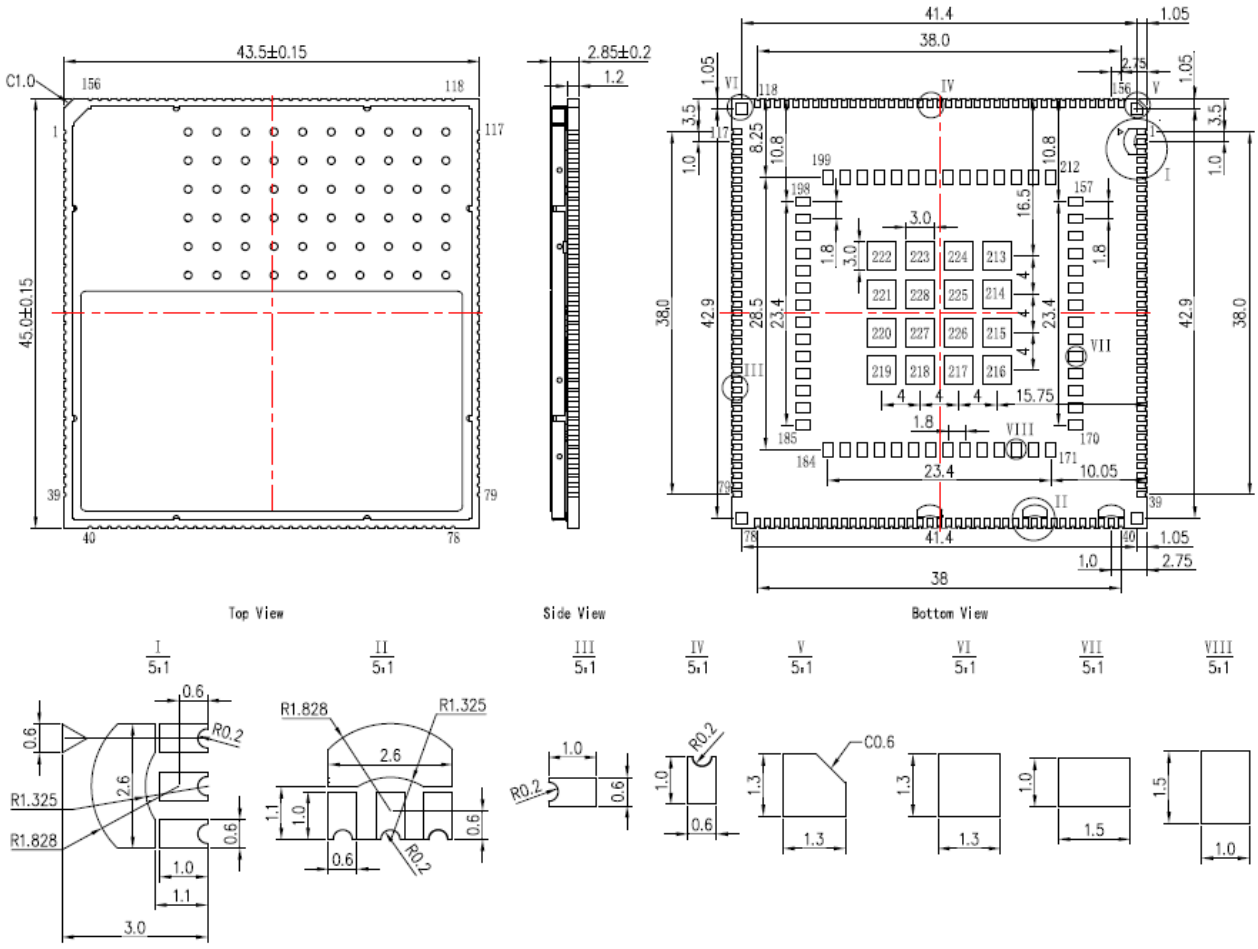

Figure 9-2 Structural Dimension

9.3 Recommended PCB Welding Plate Design

PCB soldering pad and stencil design please refer to *FIBOCOM SC820 Series SMT Design Design*.

10 Production and Storage

10.1 SMT

SMT production process parameters and related requirements please refer to *FIBOCOM SC820 Series SMT Design Guide.*

10.2 Carrier and storage

Carrier and storage please refer to *FIBOCOM SC820 Series SMT Design Guide*.

A. Acronyms

Table A-1 Acronyms

Term	Description
bps	Bits Per Second
CS	Coding Scheme
DRX	Discontinuous Reception
EGSM	Extended GSM900 Band
FDD	Frequency Division Duplexing
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile Communications
LTE	Long Term Evolution
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RMS	Root Mean Square
RTC	Real Time Clock
Rx	Receive
SMS	Short Message Service
TX	Transmitting Direction
TDD	Time Division Duplexing

Term	Description
UART	Universal Asynchronous Receiver & Transmitter
(U)SIM	(Universal) Subscriber Identity Module
WCDMA	Wideband Code Division Multiple Access

B. GPRS Encoding Scheme

Table B-1 GPRS Encoding Scheme

Encoding method	CS-1	CS-2	CS-3	CS-4
Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl. USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

C. GPRS Multislot

In the GPRS standard, 29 types of GPRS multislot modes are defined and can be used by mobile stations. The multislot class defines the maximum rate of uplink and downlink. The expression is 3+1 or 2+2, the first number represents the number of downlink timeslots and the second number represents the number of uplink timeslots. Active timeslot represents the total number of timeslots that the GPRS device can use for both uplink and downlink communications.

Table C-1 Multilevel Multislot Allocation

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
33	5	4	6

D. EDGE Modulation and Encoding Method

Table D-1 EDGE Modulation and Encoding Method

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1	GMSK	/	9.05kbps	18.1kbps	36.2kbps
CS-2	GMSK	/	13.4kbps	26.8kbps	53.6kbps
CS-3	GMSK	/	15.6kbps	31.2kbps	62.4kbps
CS-4	GMSK	/	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	C	8.80kbps	17.6kbps	35.2kbps
MCS-2	GMSK	B	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	C	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	B	22.4kbps	44.8kbps	89.6kbps
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	B	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps