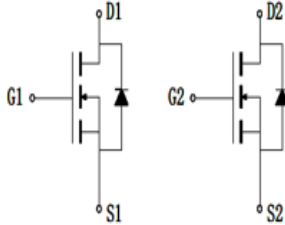
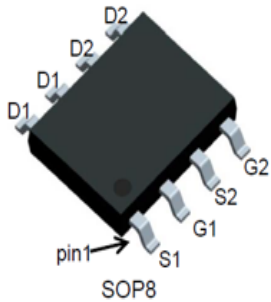


N-Channel Enhancement Mode Field Effect Transistor



SOP-8

Product Summary

- V_{DS} 60V
- I_D 5.0A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) <44mohm
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <49mohm

General Description

- Trench Power MV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching

Applications

- Battery protection
- Load switch
- Power management

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

| Parameter | | Symbol | Maximum | Unit |
|--|---------------------------------------|-----------------|----------|---------------------------|
| Drain-source Voltage | | V_{DS} | 60 | V |
| Gate-source Voltage | | V_{GS} | ± 20 | V |
| Drain Current | $T_A=25^\circ\text{C}$ @ Steady State | I_D | 5.0 | A |
| | $T_A=70^\circ\text{C}$ @ Steady State | | 4.0 | |
| Pulsed Drain Current ^A | | I_{DM} | 25 | A |
| Total Power Dissipation @ $T_A=25^\circ\text{C}$ | | P_D | 3.1 | W |
| Thermal Resistance Junction-to-Ambient @ Steady State ^B | | $R_{\theta JA}$ | 40.3 | $^\circ\text{C}/\text{W}$ |
| Junction and Storage Temperature Range | | T_J, T_{STG} | -55~+150 | $^\circ\text{C}$ |

■ Ordering Information (Example)

| PREFERRED P/N | PACKING CODE | Marking | MINIMUM PACKAGE(pcs) | INNER BOX QUANTITY(pcs) | OUTER CARTON QUANTITY(pcs) | DELIVERY MODE |
|---------------|--------------|---------|----------------------|-------------------------|----------------------------|---------------|
| YJS05N06A | F2 | Q05N06 | 4000 | 8000 | 64000 | 13" reel |



YJS05N06A

■ Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---------------------------------------|--------------|--|-----|------|-----------|------------|
| Static Parameter | | | | | | |
| Drain-Source Breakdown Voltage | BV_{DSS} | $V_{GS}=0V, I_D=250\mu A$ | 60 | | | V |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS}=60V, V_{GS}=0V$ | | | 1 | μA |
| Gate-Body Leakage Current | I_{GSS} | $V_{GS}=\pm 20V, V_{DS}=0V$ | | | ± 100 | nA |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}, I_D=250\mu A$ | 1.0 | 1.5 | 2.5 | V |
| Static Drain-Source On-Resistance | $R_{DS(on)}$ | $V_{GS}=10V, I_D=5.0A$ | | 35 | 44 | m Ω |
| | | $V_{GS}=4.5V, I_D=4.0A$ | | 39 | 49 | |
| Diode Forward Voltage | V_{SD} | $I_S=5.0A, V_{GS}=0V$ | | 0.8 | 1.2 | V |
| Maximum Body-Diode Continuous Current | I_S | | | | 5.0 | A |
| Dynamic Parameters | | | | | | |
| Input Capacitance | C_{iss} | $V_{DS}=30V, V_{GS}=0V, f=1MHz$ | | 1018 | | pF |
| Output Capacitance | C_{oss} | | | 70 | | |
| Reverse Transfer Capacitance | C_{rss} | | | 62 | | |
| Switching Parameters | | | | | | |
| Total Gate Charge | Q_g | $V_{GS}=10V, V_{DS}=30V, I_D=10A$ | | 26 | | nC |
| Gate Source Charge | Q_{gs} | | | 5.4 | | |
| Gate Drain Charge | Q_{gd} | | | 6.5 | | |
| Reverse Recovery Charge | Q_{rr} | $I_F=20A, di/dt=500A/us$ | | 11.7 | | ns |
| Reverse Recovery Time | t_{rr} | | | 23 | | |
| Turn-on Delay Time | $t_{D(on)}$ | $V_{GS}=10V, V_{DD}=30V, I_D=2A, R_L=1\Omega$ $R_{GEN}=3\Omega$ | | 10 | | ns |
| Turn-on Rise Time | t_r | | | 20 | | |
| Turn-off Delay Time | $t_{D(off)}$ | | | 29 | | |
| Turn-off Fall Time | t_f | | | 21 | | |

A. Pulse Test: Pulse Width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

B. $R_{\theta JA}$ is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JL}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

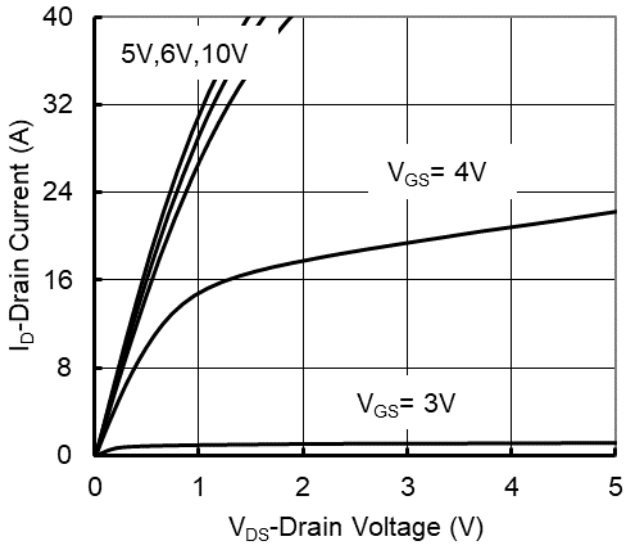


Figure 1. Output Characteristics

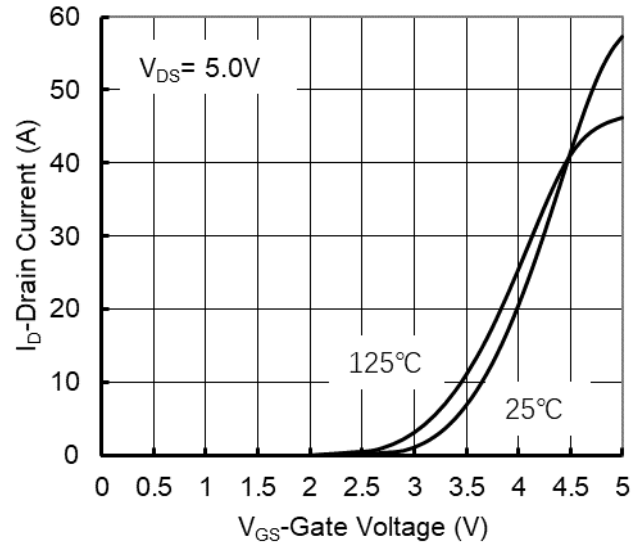


Figure 2. Transfer Characteristics

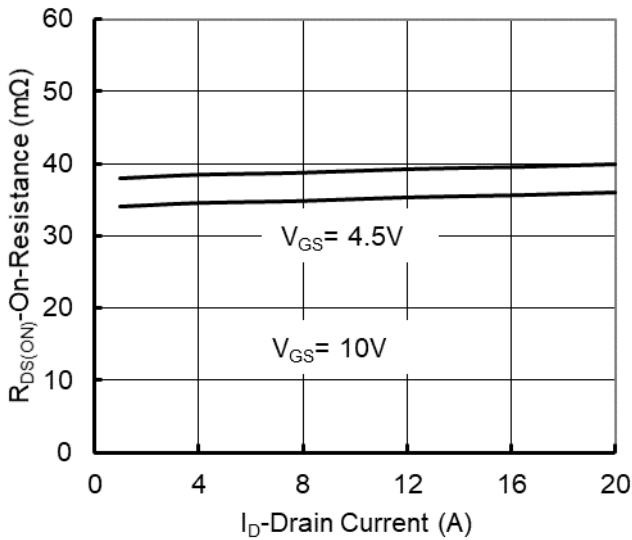


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

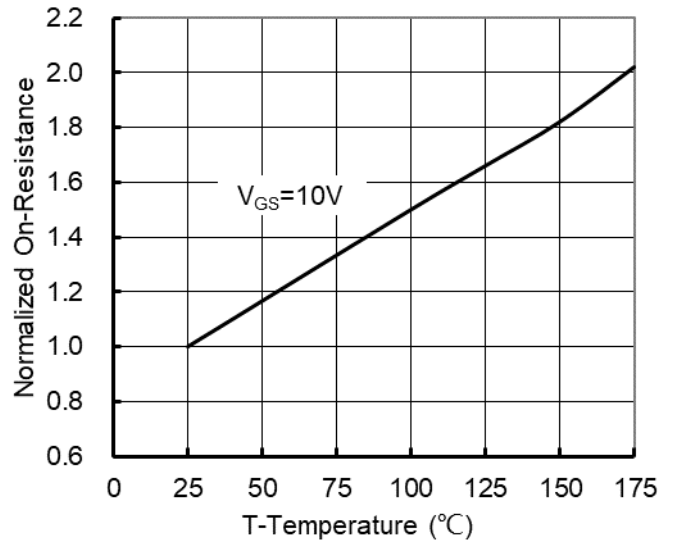


Figure 4. On-Resistance vs. Junction Temperature

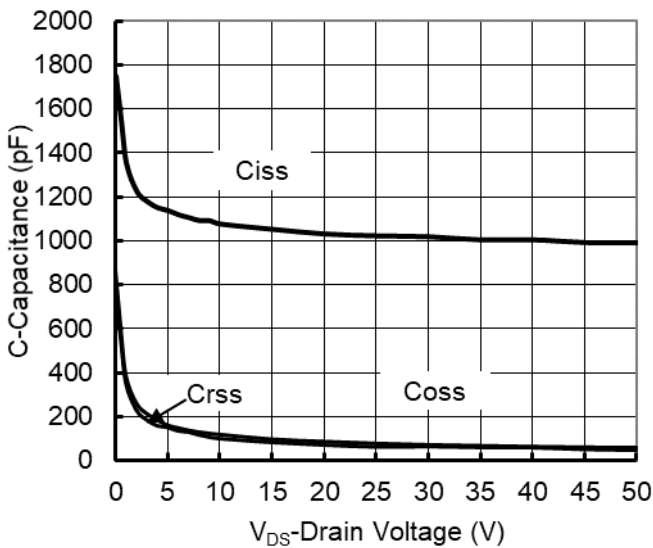


Figure 5. Capacitance Characteristics

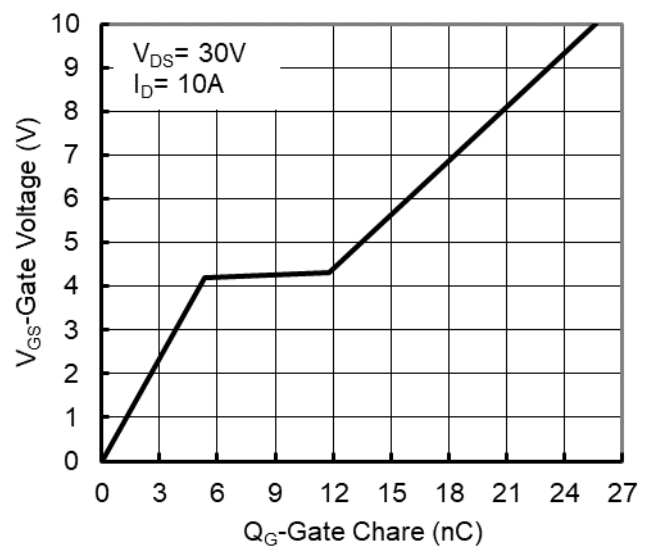


Figure 6. Gate Charge



YJS05N06A

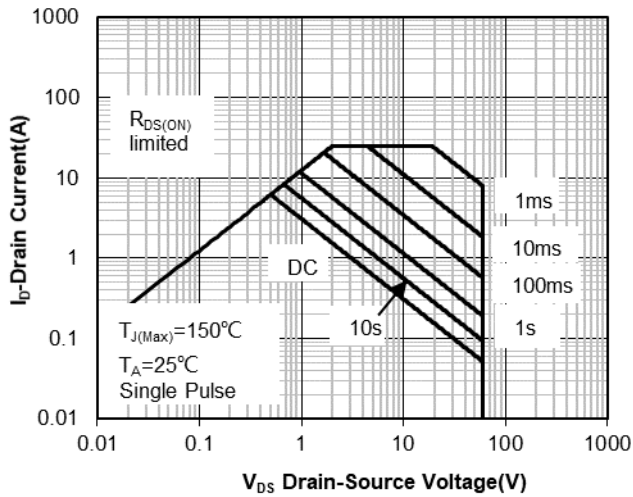


Figure 7. Safe Operation Area

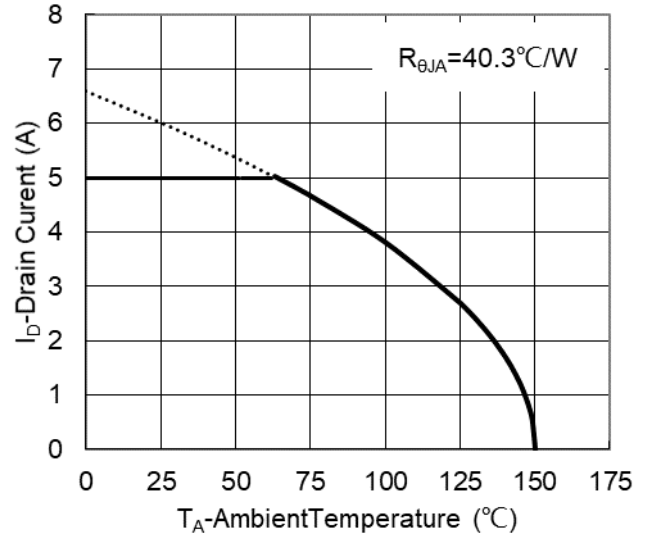


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

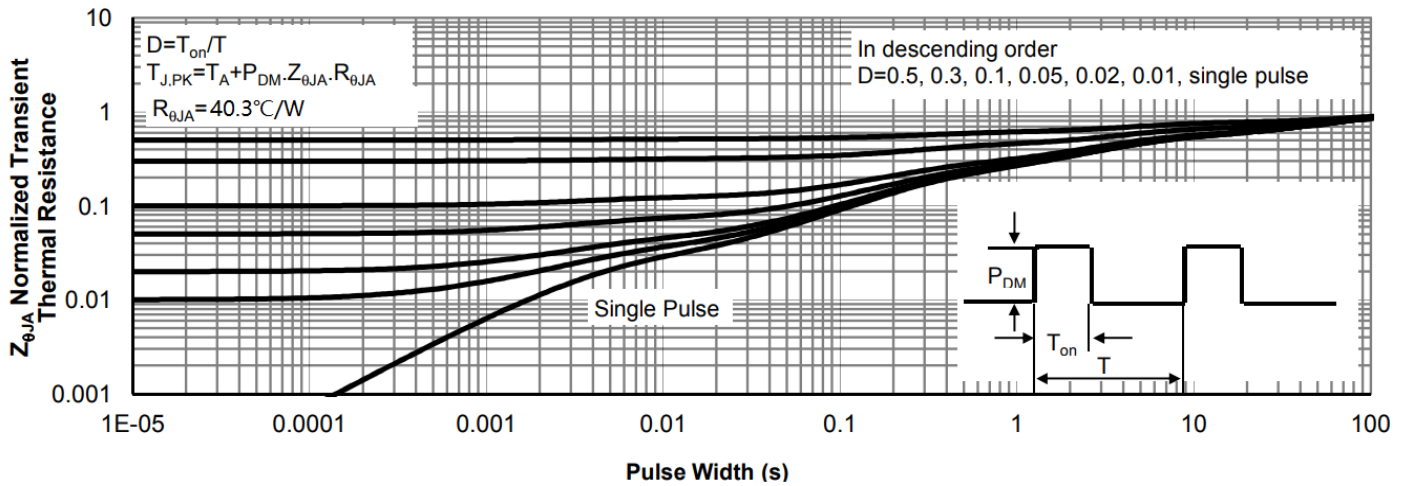
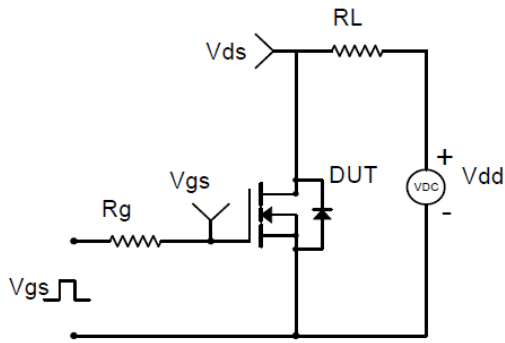
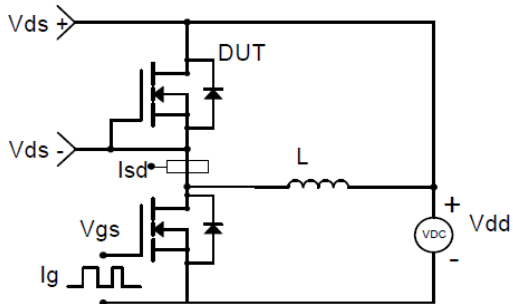


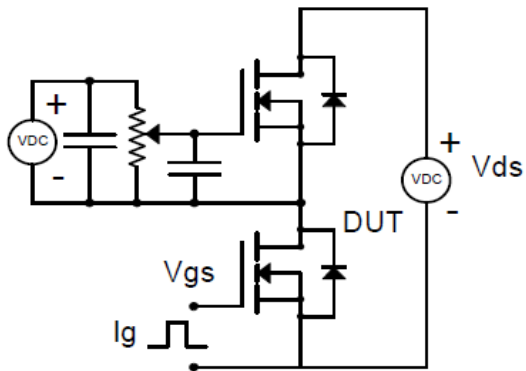
Figure 9. Normalized Maximum Transient Thermal Impedance



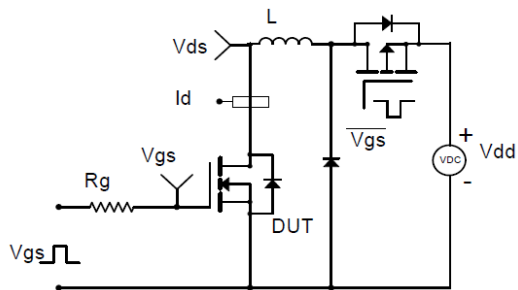
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform

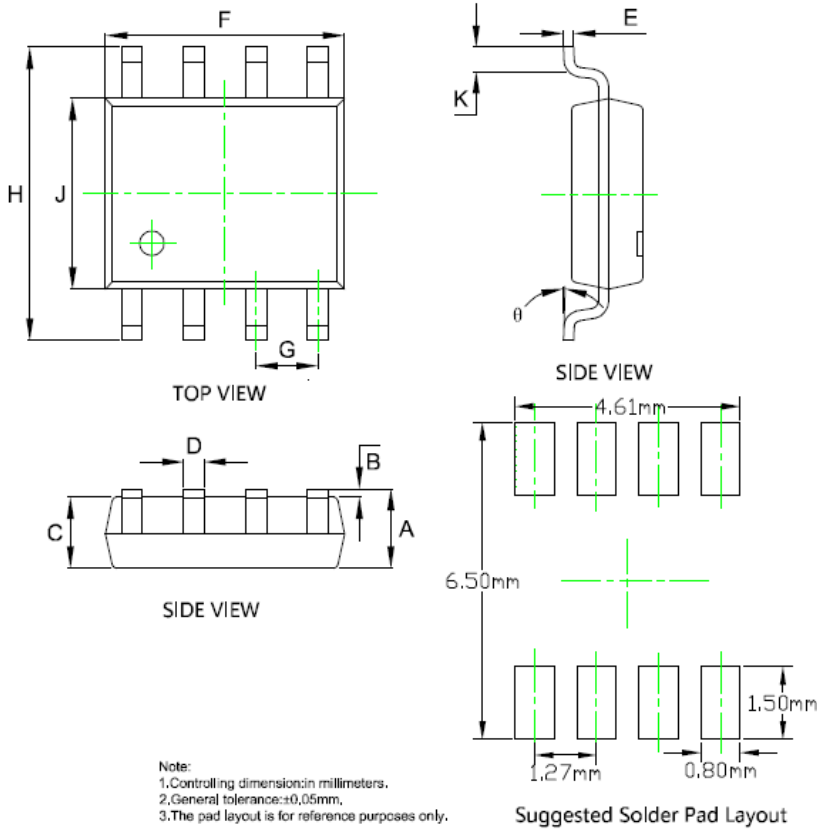


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



YJS05N06A

■SOP-8 Package information



| SYMBOL | DIMENSIONS | | | |
|--------|------------|-------|------------|-------|
| | INCHES | | Millimeter | |
| | MIN. | MAX. | MIN. | MAX. |
| A | 0.053 | 0.069 | 1.350 | 1.750 |
| B | 0.004 | 0.010 | 0.100 | 0.250 |
| C | 0.053 | 0.061 | 1.350 | 1.550 |
| D | 0.013 | 0.020 | 0.330 | 0.510 |
| E | 0.007 | 0.010 | 0.170 | 0.250 |
| F | 0.189 | 0.197 | 4.800 | 5.000 |
| G | 0.050BSC | | 1.270BSC | |
| H | 0.228 | 0.244 | 5.800 | 6.200 |
| J | 0.150 | 0.157 | 3.800 | 4.000 |
| K | 0.016 | 0.050 | 0.400 | 1.270 |
| θ | 0° | 8° | 0° | 8° |



YJS05N06A

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