

SCM3725ASA/SCM3728ASA Dual-Channel Digital Isolators

Features

- 3 V to 5.5 V level translation
- High common-mode transient immunity: 75 kV/μs typical
- High robustness to radiated and conducted noise
- High ESD rating
- Ultra low power consumption 0.58mA/channel(1Mbps)
- Wide temperature range: -40°C ~ 125°C
- Isolation voltages: AC 3000Vrms
- High data rate: 10Mbps

Package



Mechanical package: SOP-8
(see "Ordering information" for details).

Applications

- General-purpose multichannel isolation
- Industrial field bus isolation

Functional

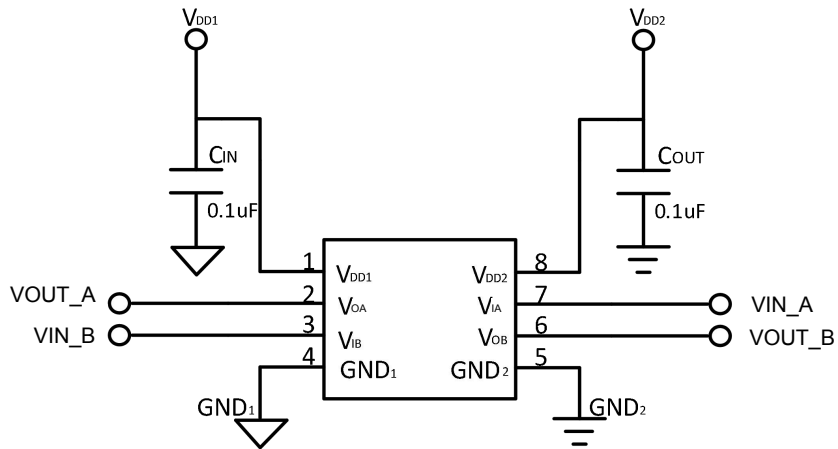
The SCM3725ASA/SCM3728ASA digital isolators by using matured standard semiconductor CMOS technology and Capacitance pulse isolation technology, these isolation components provide outstanding performance characteristics and reliability superior to alternatives such as optocoupler devices and other integrated isolators.

Capacitance pulse isolation technology is a new generation digital isolator technology . It uses the principle of capacitor voltage divider to transmit voltage signal directly cross the isolator capacitor without signal modulation and demodulation.

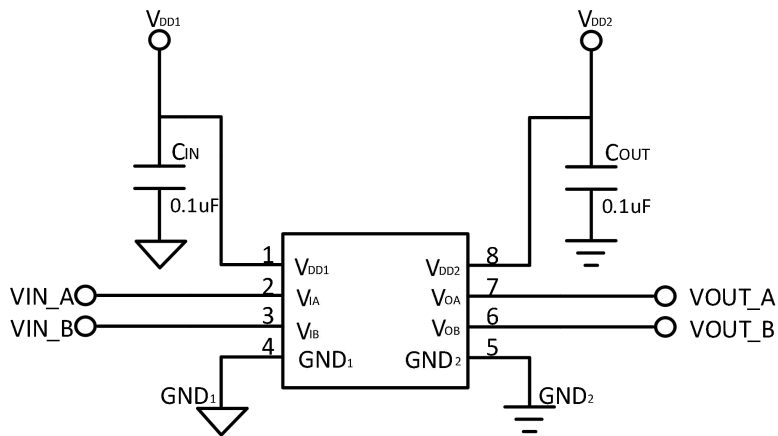
The SCM3725ASA/SCM3728ASA isolator data channels are independent and different models have different transmission directions with a withstand voltage rating of 3 kV rms and the data rate from DC up to 10Mbps . The devices operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier. The fail-safe state is available in which the outputs transition to a preset state when the input power supply is not applied.

Product model

Model	Power supply range (V)	Data rate	Channel number	Output channel number	Withstand voltage(kV rms)	Default output	Package option	Pin number
SCM3725ASA	3.0~5.5	10Mbps	2	1	3	high	SOP	8
SCM3728ASA	3.0~5.5	10Mbps	2	2	3	low	SOP	8



Typical Circuit: 1 SCM3725ASA Application Diagram



Typical Circuit: 2 SCM3728ASA Application Diagram

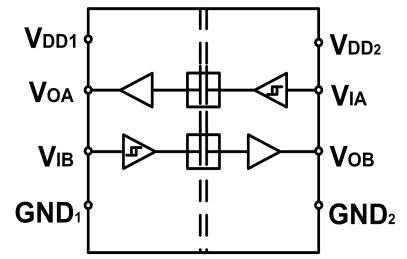
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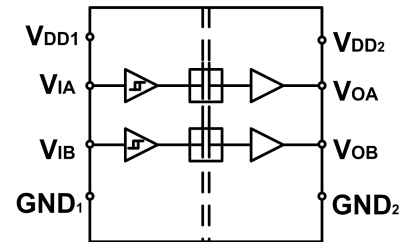
Pin Connection



Internal Block



SCM3725ASA



SCM3728ASA

Function table

Vix Input ¹	VDDI State ¹	VDDO State ¹	Default Low	Default High	Test Conditions /Comments
			VOx Output ¹	VOx Output ¹	
Low	Powered ²	Powered ²	Low	Low	Normal operation
High	Powered ²	Powered ²	High	High	Normal operation
Open	Powered ²	Powered ²	Low	High	Default output
Don't Care ⁴	Unpowered ³	Powered ²	Low	High	Default output ⁵
Don't Care ⁴	Powered ²	Unpowered ³	High Impedance	High Impedance	

Notes:

1Vix/VOx are the input/output signals of a given channel (A or B). VDDI/VDDO are the supply voltages on the input/output signal sides of this given channel.

2Powered means VDDx ≥ 2.9 V

3Unpowered means VDDx < 2.3V

4Input signal (Vix) must be in a low state to avoid powering the given VDDI1 through its ESD protection circuitry.

5If the VDDI goes into unpowered status, the channel outputs the default logic signal after around 1us. If the VDDI goes into powered status, the channel outputs the input status logic signal after around 3us.

Pin descriptions

SCM3725ASA		
Pin No.	Name	Description
1	VDD1	Supply Voltage for Isolator Side 1.
2	VOA	Logic Output A.
3	VIB	Logic Input B.
4	GND1	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND2	Ground 2. This pin is the ground reference for Isolator Side 2.
6	VOB	Logic Output B.
7	VIA	Logic Input A.
8	VDD2	Supply Voltage for Isolator Side 2.

SCM3725ASA		
Pin No.	Name	Description
1	VDD1	Supply Voltage for Isolator Side 1.
2	VIA	Logic Input A.
3	VIB	Logic Input B.
4	GND1	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND2	Ground 2. This pin is the ground reference for Isolator Side 2.
6	VOB	Logic Output B.
7	VOA	Logic Output A.
8	VDD2	Supply Voltage for Isolator Side 2.

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Parameter	SYMBOL	RANGE	UNIT
Supply Voltages	$V_{DD1-GND1}, V_{DD2-GND2}$	-0.5 V to +7.0 V	V
Input Voltages	V_{IA}, V_{IB}	-0.5 V to $V_{DDx} + 0.5$ V	V
Output Voltages	V_{OA}, V_{OB}	-0.5 V to $V_{DDx} + 0.5$ V	V
Average Output Current per Pin ² Side 1 Output Current	I_{O1}	-10 mA to +10 mA	mA
Average Output Current per Pin Side 2 Output Current	I_{O2}	-10 mA to +10 mA	mA
Common-Mode Transients Immunity		-150 kV/ μs to +150 kV/ μs	kV/ μs
Storage Temperature Range	T_{ST}	-65°C to +150°C	°C
Ambient Operating Temperature Range	T_A	-40°C to +125°C	°C

Notes:

1 VDDx is the side voltage power supply VDD, where x = 1 or 2.

2 See Figure9 for the maximum rated current values for various temperatures.

3 See Figure18 for Common-mode transient immunity (CMTI) measurement.

4 Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DDx}^1	3		5.5	V
High Level Input Signal Voltage	V_{IH}	$0.7 \cdot V_{DDx}^1$		V_{DDx}^1	V
Low Level Input Signal Voltage	V_{IL}	0		$0.3 \cdot V_{DDx}^1$	V
High Level Output Current	I_{OH}	-6			mA
Low Level Output Current	I_{OL}			6	mA
Maximum Data Rate		0		10	Mbps
Junction Temperature	T_J	-40		150	°C
Ambient Operating Temperature	T_A	-40		125	°C

Notes:

1 VDDx is the side voltage power supply VDD, where x = 1 or 2.

Switching Specifications						
Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Minimum Pulse Width	PW	Within pulse width distortion (PWD) limit			100	ns
Maximum Data Rate		Within PWD limit	10			Mbps
Propagation Delay Time ^{1,4}	tpHL, tpLH	The different time between 50% input signal to 50% output signal 50% @ 5VDC supply	5.5	8	12.5	ns
		@ 3.3VDC supply	6.5	9	13.5	ns
Pulse Width Distortion ⁴	PWD	The max different time between tpHL and tpLH@ 5VDC supply. And The value is tpHL - tpLH	0	0.3	0.8	ns
		@ 3.3VDC supply	0	0.3	0.8	ns
Part to Part Propagation Delay Skew ⁴	tPSK	The max different propagation delay time between any two devices at the same temperature, load and voltage @ 5VDC supply			1	ns
		@ 3.3VDC supply			1	ns
Channel to Channel Propagation Delay Skew ⁴	tCSK	The max amount propagation delay time differs between any two output channels in the single device @ 5VDC supply.		0	1	ns
		@ 3.3VDC supply		0	0.8	ns
Output Signal Rise/Fall Time ⁴	t _r /t _f	10% to 90% signal terminated 50 Ω, See figure15.		1.5		ns
Dynamic Input Supply Current per Channel	IDDI (D)	Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 5VDC Supply		9		μA /Mbps
Dynamic Output Supply Current per Channel	IDDO (D)	Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 5VDC Supply		38		μA /Mbps
Dynamic Input Supply Current per Channel	IDDI (D)	Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 3.3VDC Supply		5		μA /Mbps
Dynamic Output Supply Current per Channel	IDDO (D)	Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 3.3VDC Supply		23		μA /Mbps
Common-Mode Transient Immunity ³	CMTI	V _{IN} = V _{DDx} ² or 0V, V _{CM} = 1000 V.		75		kV/μs
Jitter		See the Jitter Measurement section		120		Ps p-p
		See the Jitter Measurement section		20		Ps rms
ESD (HBM - Human body model)	ESD	All pins		±8		kV
DC Specifications						
Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Rising Input Signal Voltage Threshold	V _{IT+}			0.6*V _{DDx}	0.7*V _{DDx}	V
Falling Input Signal Voltage Threshold	V _{IT-}		0.3* V _{DDx}	0.4* V _{DDx}		V
High Level Output Voltage	VOH	-20 μA output current	V _{DDx} - 0.1	V _{DDx}		V
		-2 mA output current	V _{DDx} - 0.2	V _{DDx} - 0.1		V
Low Level Output Voltage	VOL	20 μA output current		0	0.1	V
		2 mA output current		0.1	0.2	V
Input Current per Signal Channel	I _{IN}	0 V ≤ Signal voltage ≤ V _{DDx} ¹	-10	0.5	10	μA
V _{DDx} ¹ Undervoltage Rising Threshold	VDDxUV+		2.45	2.65	2.9	V
V _{DDx} ¹ Undervoltage Falling Threshold	VDDxUV-		2.3	2.5	2.75	V
V _{DDx} ¹ Hysteresis	VDDxUVH			0.15		V
Quiescent Supply Current						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCM3725ASA Quiescent Supply Current @ 5VDC Supply	IDD1 (Q)	0V Input signal	419	524	681	μA
	IDD2 (Q)	0V Input signal	419	524	681	μA
	IDD1 (Q)	5V Input signal	436	545	709	μA
	IDD2 (Q)	5V Input signal	436	545	709	μA
SCM3725ASA Quiescent Supply Current@ 3.3VDC Supply	IDD1 (Q)	0V Input signal	414	518	673	μA
	IDD2 (Q)	0V Input signal	414	518	673	μA
	IDD1 (Q)	3.3V Input signal	408	510	663	μA
	IDD2 (Q)	3.3V Input signal	408	510	663	μA
SCM3728ASA	IDD1 (Q)	0V Input signal	64	80	104	μA

Quiescent Supply Current @ 5VDC Supply	IDD2 (Q)	0V Input signal	781	976	1269	μA
	IDD1 (Q)	5V Input signal	158	197	256	μA
	IDD2 (Q)	5V Input signal	738	923	1200	μA
SCM3728ASA Quiescent Supply Current@ 3.3VDC Supply	IDD1 (Q)	0V Input signal	63	79	103	μA
	IDD2 (Q)	0V Input signal	772	965	1255	μA
	IDD1 (Q)	3.3V Input signal	116	145	189	μA
	IDD2 (Q)	3.3V Input signal	709	886	1152	μA

Total Supply Current vs. Data Throughput (CL = 0 pF)
 $V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3VDC \pm 10\%$ or $5VDC \pm 10\%$, $T_A = 25^\circ C$, $CL = 0$ pF, unless otherwise noted.

Parameter	Symbol	150Kbps			1Mbps			10Mbps			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SCM3725ASA Supply Current @ 5VDC	IDD1		0.54	0.81		0.58	0.86		0.97	1.60	mA
	IDD2		0.54	0.81		0.58	0.86		0.97	1.60	mA
SCM3725ASA Supply Current @ 3.3VDC	IDD1		0.52	0.78		0.54	0.81		0.77	1.20	mA
	IDD2		0.52	0.78		0.54	0.81		0.77	1.20	mA
SCM3728ASA Supply Current @ 5VDC	IDD1		0.14	0.21		0.15	0.22		0.24	0.36	mA
	IDD2		0.95	1.43		1.02	1.52		1.76	2.63	mA
SCM3728ASA Supply Current @ 3.3VDC	IDD1		0.11	0.17		0.12	0.17		0.18	0.27	mA
	IDD2		0.93	1.40		0.97	1.46		1.43	2.14	mA

INSULATION AND SAFETY RELATED SPECIFICATIONS

Insulation Specifications					
Parameter	Symbol	Value		Unit	Test Conditions/Comments
		SCM3725ASA/SCM3728ASA			
Rated Dielectric Insulation Voltage		3000		V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (CLR)	4		mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (CRP)	4		mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		11		μm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400		V	DIN IEC 112/VDE 0303 Part 1
Material Group		II			Material Group (DIN VDE 0110, 1/89, Table 1)

PACKAGE CHARACTERISTICS

Package Characteristics					
Parameter	Symbol	Typical Value		Unit	Test Conditions/Comments
		SCM3725ASA/SCM3728ASA			
Resistance (Input to Output)	RI-O	10^{11}		Ω	
Capacitance (Input to Output)	CI-O	0.6		pF	@1MHz
Input Capacitance ²	C _i	3		pF	@1MHz
IC Junction to Ambient Thermal Resistance	θ _{JA}	100		°C/W	Thermocouple located at center of package underside

REGULATORY INFORMATION

See the Table and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

Regulatory	SCM3725ASA/SCM3728ASA
UL	Recognized under UL 1577 Component Recognition Program ¹ Single Protection, 3000 V rms Isolation Voltage
CSA	Approved under CSA Component Acceptance Notice 5A CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2: Basic insulation at 500 V rms (707 V peak)

	Reinforced insulation at 250 V rms (353 V peak)
VDE	DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 ² Basic insulation, $V_{IORM} = 707$ V peak, $V_{IOSM} = 4615$ V peak
CQC	Certified under CQC11-471543-2012 GB4943.1-2011 Basic insulation at 500 V rms (707 V peak) working voltage Reinforced insulation at 250 V rms (353 V peak)

INSULATION CHARACTERISTICS

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
			SCM3725ASA/SCM3728ASA	
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to III	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	707	V peak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1326	V peak
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1061	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		849	V peak
Highest Allowable Overvoltage		V_{IOTM}	4200	V peak
Surge Isolation Voltage Basic	Basic insulation, $1.2 \mu s$ rise time, $50 \mu s$, 50% fall time	V_{IOSM}	4615	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Maximum Junction Temperature		T_s	150	$^{\circ}C$
Total Power Dissipation at $25^{\circ}C$		P_s	1.56	W
Insulation Resistance at T_s	$V_{IO} = 800$ V	R_s	$>10^9$	Ω

Typical Performance Curves

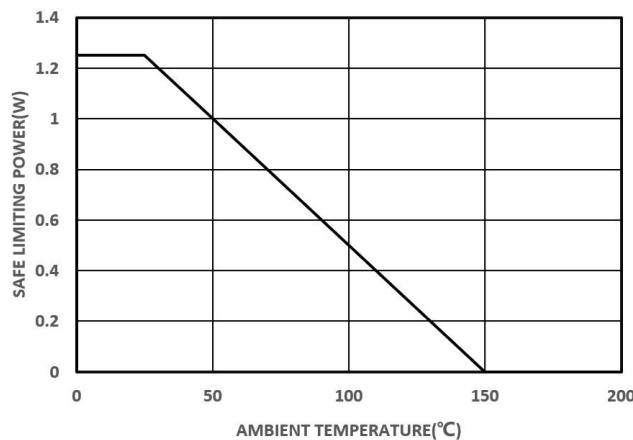
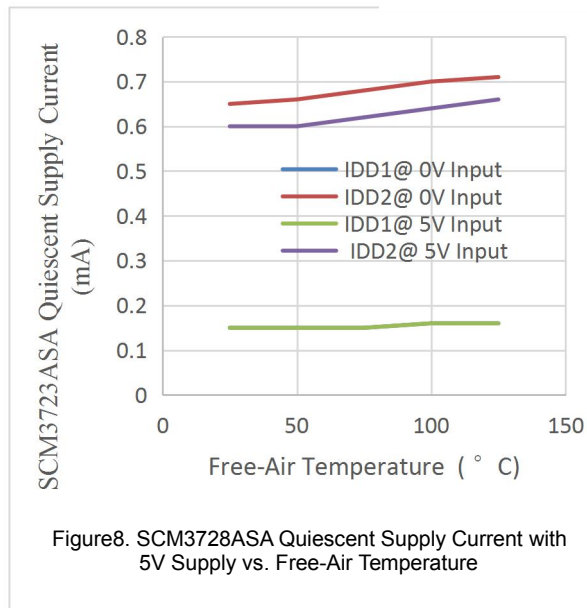
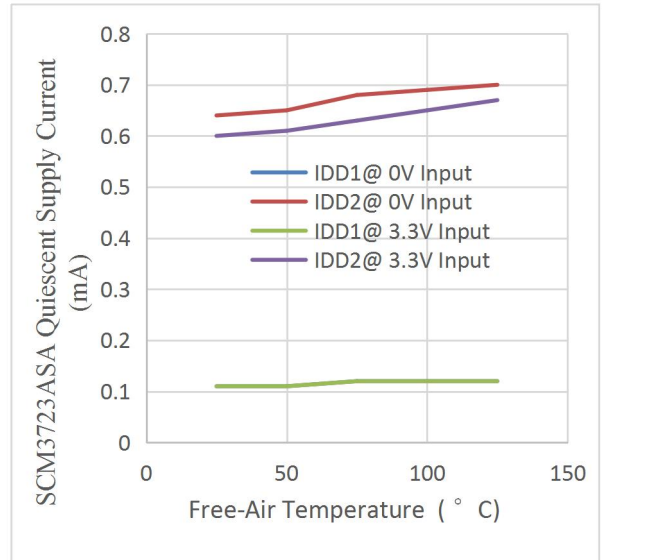
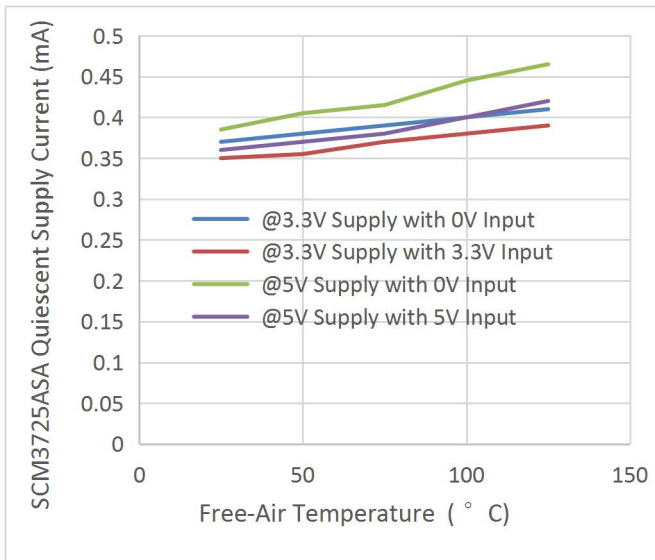
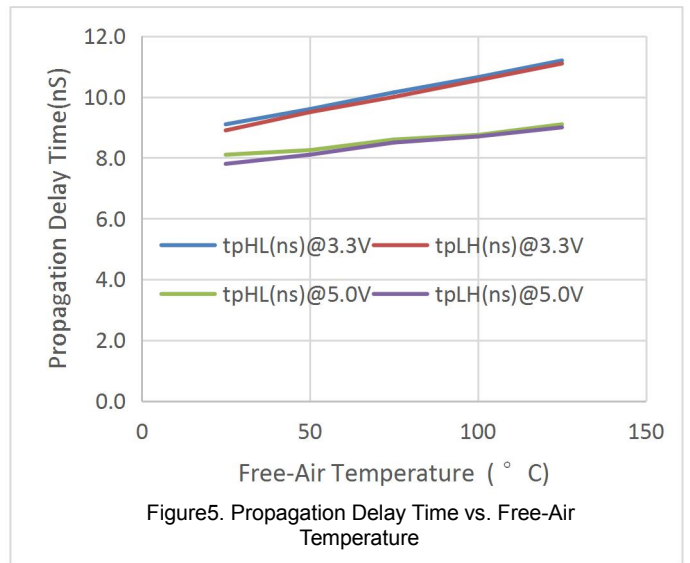
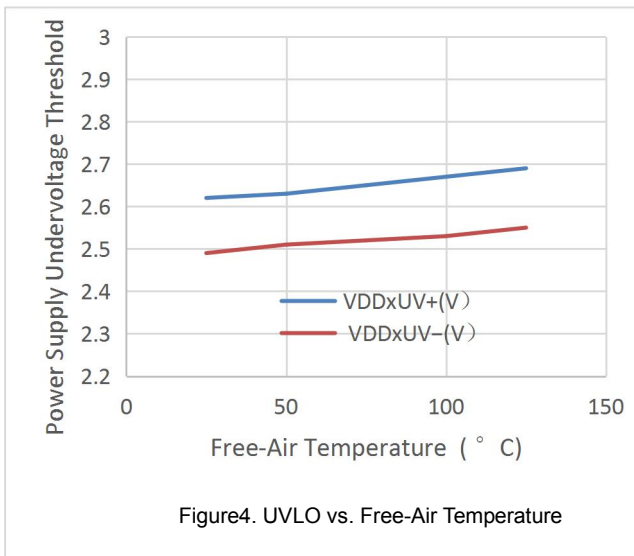


Figure3. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per VDE



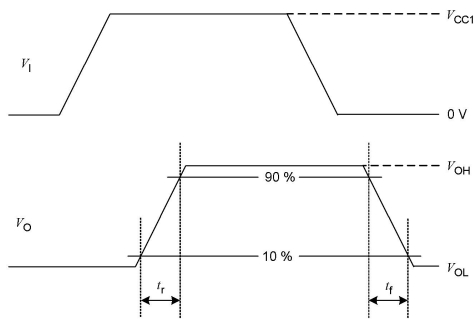


Figure9. Transition time waveform measurement

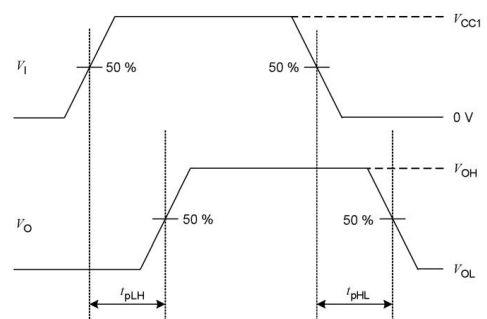


Figure10. Propagation delay time waveform measurement

APPLICATIONS INFORMATION

OVERVIEW

The SCM3725ASA/SCM3728ASA are digital isolators product family based on unique Capacitance pulse isolation technology. Capacitance pulse isolation technology is a new generation digital isolator technology. It uses the principle of capacitor voltage divider to transmit signal directly cross the isolator capacitor without signal modulation and demodulation. Compare to the traditional Opto-couple technology, icoupler technology, OOK technology, Capacitance pulse isolation technology is a more essential and concise isolation signal transmit technology which leads to greatly simplification on circuit design and therefore significantly improves device performance, such as lower power consumption, faster speed, enhanced anti-interference ability, lower noise.

By using maturated standard semiconductor CMOS technology and the innovative Capacitance pulse isolation technology design, these isolation components provide outstanding performance characteristics and reliability superior to alternatives such as optocoupler devices and other integrated isolators. The SCM3725ASA/SCM3728ASA isolator data channels are independent and are available in a variety of configurations with a withstand voltage rating of 1.5 kV rms to 6.0 kV rms and the data rate from DC up to 10Mbps (see the Ordering Guide).

The SCM3725ASA/SCM3728ASA are the outstanding 150Kbps dual-channel digital isolators with the enhanced ESD capability. the devices transmit data across an isolation barrier by layers of silicon dioxide isolation.

The devices operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, offering voltage translation of 3.3 V and 5 V logic.

The SCM3725ASA/SCM3728ASA have very low propagation delay and high speed. The input/output design techniques allow logic and supply voltages over a wide range from 3.0 V to 5.5 V, offering voltage translation of 3.3 V and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference.

PCB LAYOUT

The low-ESR ceramic bypass capacitors must be connected between V_{DD1} and GND_1 and between V_{DD2} and GND_2 . The bypass capacitors are placed on the PCB as close to the isolator device as possible. The recommended bypass capacitor value is between 0.1 μF and 10 μF . To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy.

Avoid reducing the isolation capability, Keep the space underneath the isolator device free from metal such as planes, pads, traces and vias.

To minimize the impedance of the signal return loop, keep the solid ground plane directly underneath the high-speed signal path, the closer the better. The return path will couple between the nearest ground plane to the signal path. Keep suitable trace width for controlled impedance transmission lines interconnect.

To reduce the rise time degradation, keep the length of input/output signal traces as short as possible, and route low inductance loop for the signal path and It's return path.

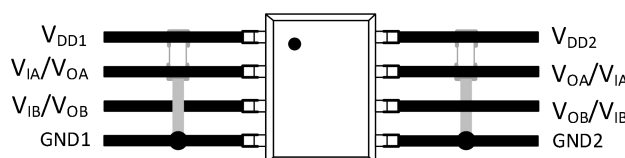


Figure 11.Recommended Printed Circuit Board Layout

JITTER MEASUREMENT

The eye diagram shown in the figure 9 provides the jitter measurement result for the SCM3725ASA/SCM3728ASA. The Keysight 81160A pulse function arbitrary generator works as the data source for the SCM3725ASA/SCM3728ASA, which generates 10Mbps pseudo random bit sequence (PRBS). The Keysight DSOS104A digital storage oscilloscope captures the SCM3725ASA/SCM3728ASA output waveform and recovers the eye diagram with the SDA jitter tools and eye diagram analysis tools. The result shows a typical measurement 120ps p-p jitter.

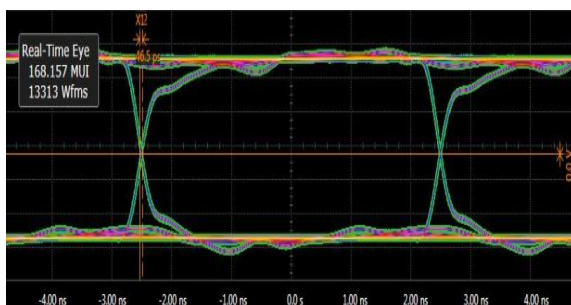


Figure 12. SCM3725ASA/SCM3728ASA Eye Diagram

CMTI MEASUREMENT

To measure the Common-Mode Transient Immunity (CMTI) of SCM3725ASA/SCM3728ASA isolator under specified common-mode pulse magnitude (VCM) and specified slew rate of the common-mode pulse (dVCM/dt) and other specified test or ambient conditions, The common-mode pulse generator (G1) will be capable of providing fast rising and falling pulses of specified magnitude and duration of the common-mode pulse (VCM) and the maximum common-mode slew rates (dVCM/dt) can be applied to SCM3725ASA/SCM3728ASA isolator coupler under measurement. The common-mode pulse is applied between one side ground GND1 and the other side ground GND2 of SCM3725ASA/SCM3728ASA isolator and shall be capable of providing positive transients as well as negative transients.

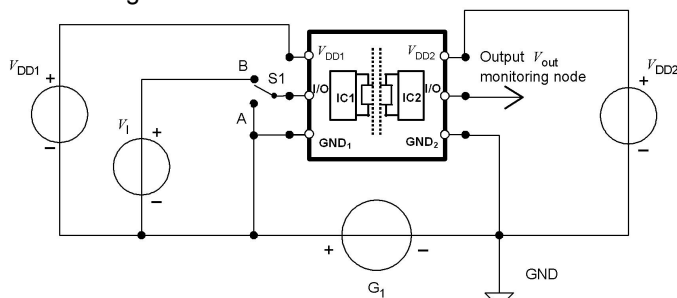


Figure 13. Common-mode transient immunity (CMTI) measurement

Ordering Information

Part number	Temperature Range	Withstand Voltage Rating (kV rms)	Package	Number of pins	Product Marking	Tape & Reel
SCM3725ASA	-40°C ~ +125°C	3	SOP	8	SCM3725ASA YM	4K/REEL
SCM3728ASA	-40°C ~ +125°C	3	SOP	8	SCM3728ASA YM	4K/REEL

Product marking and date code

SCM3401XYZ:

(1) SCM3401 = Product designation.

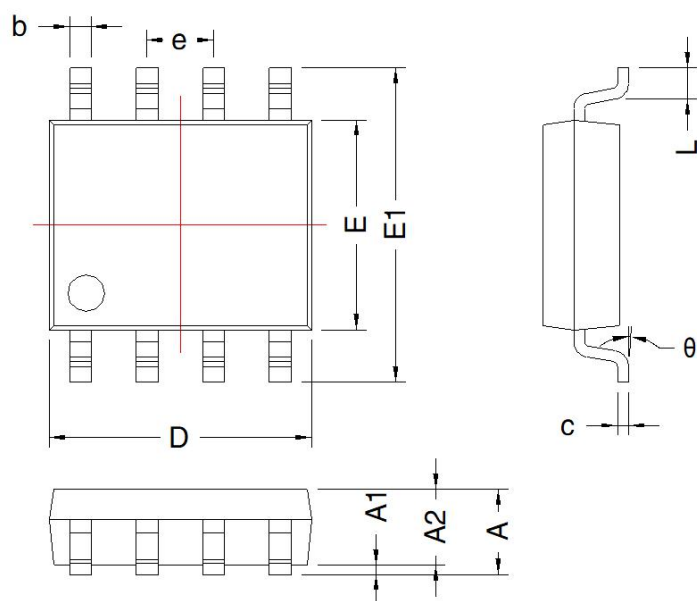
(2) X = Version code information (A-Z).

(3) Y = Packaging definition code; S for SOP package,

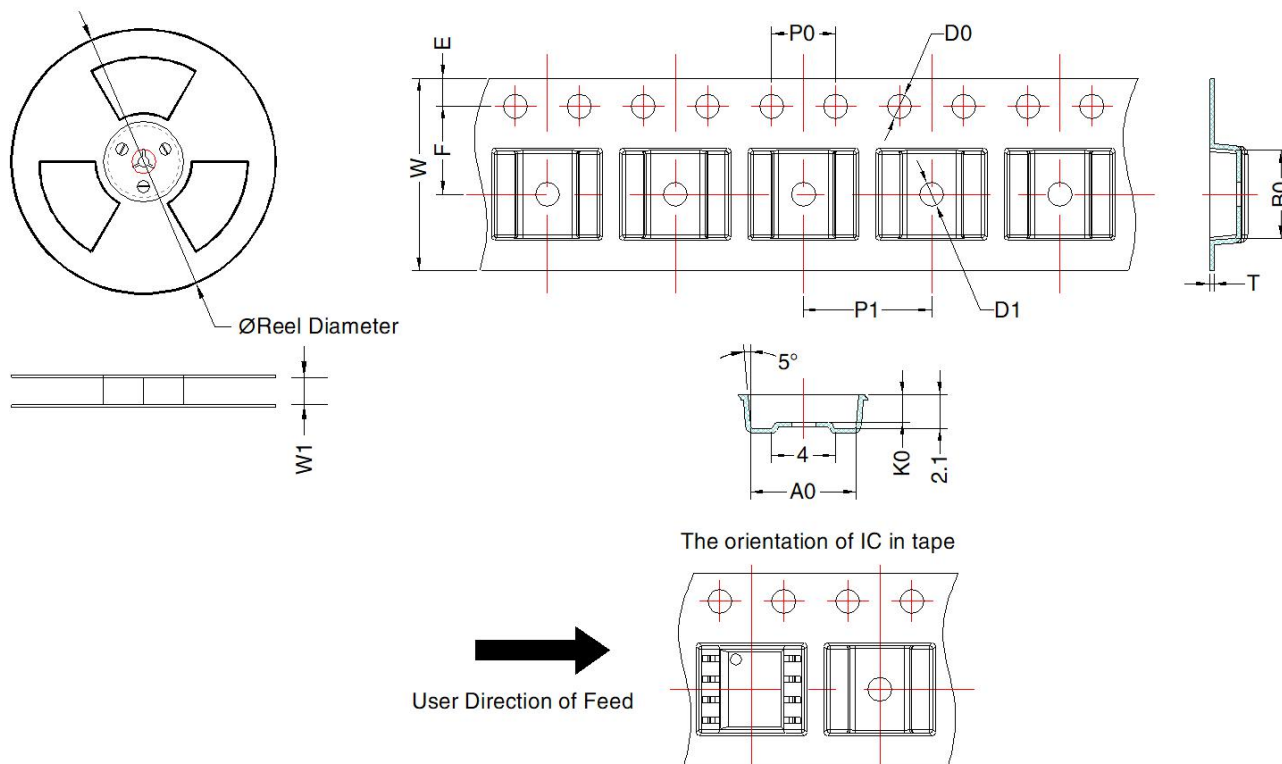
(4) Z = Operating temperature range (C = 0°C to +70°C, I = -40°C to +85°C, A = -40°C to +125°C, M = -55°C to +125°C).

(5) YM = Date code for product traceability; Y = code for production year; M = code for production month.

THIRD ANGLE PROJECTION 



SOIC-8				
Mark	Dimension(mm)		Dimension(inch)	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.1	0.25	0.004	0.010
A2	1.3	1.5	0.005	0.059
D	4.8	5.0	0.189	0.197
E	3.8	4.0	0.150	0.157
E1	5.8	6.2	0.228	0.244
L	0.45	0.8	0.018	0.031
b	0.38	0.47	0.015	0.018
e	1.27TYP		0.05TYP	
c	0.17	0.25	0.007	0.001
theta	0°	8°	0°	8°



Device	Package Type	MPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	T (mm)	W (mm)	E (mm)	F (mm)	P1 (mm)	P0 (mm)	D0 (mm)	D1 (mm)
SCM3725ASA	SOIC-8	4000	330.0	12.4	6.6±0.1	5.5±0.1	1.7±0.1	0.3±0.05	12.0±0.3	1.75±0.1	5.5±0.1	8±0.1	4±0.1	1.5±0.1	1.5±0.1

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