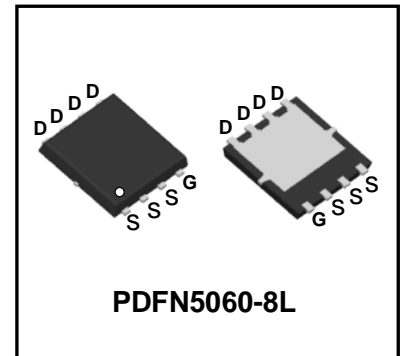


## 100V N-Channel Enhancement Mode Power MOSFET

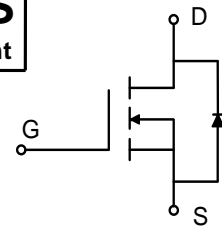
### Description

WMB080N10LG2 uses Wayon's 2<sup>nd</sup> generation power trench MOSFET technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance. This device is well suited for high efficiency fast switching applications.



### Features

- $V_{DS} = 100V$ ,  $I_D = 74A$ (Silicon Limited)  
 $R_{DS(on)} < 8m\Omega @ V_{GS} = 10V$   
 $R_{DS(on)} < 10.5m\Omega @ V_{GS} = 4.5V$
- Green Device Available
- 100% EAS Guaranteed
- Optimized for High Speed Smooth Switching



### Applications

- Hard Switching and High Speed Circuit
- DC/DC Conversion
- Synchronous Rectification in SMPS

### Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Drain-Source Voltage		$V_{DS}$	100	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>1</sup> (Silicon Limited)	$T_C=25^\circ C$	$I_D$	74	A
	$T_C=100^\circ C$		47	
Pulsed Drain Current <sup>2</sup>		$I_{DM}$	260	A
Single Pulse Avalanche Energy <sup>3</sup>		<b>EAS</b>	231	mJ
Avalanche Current		$I_{AS}$	34	A
Total Power Dissipation <sup>4</sup>	$T_C=25^\circ C$	<b>P<sub>D</sub></b>	84	W
Operating Junction and Storage Temperature Range		<b>T<sub>J</sub> , T<sub>STG</sub></b>	-55 to 150	$^\circ C$

### Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient <sup>1</sup>	<b>R<sub>θJA</sub></b>	50	$^\circ C/W$
Thermal Resistance from Junction-to-Case <sup>1</sup>	<b>R<sub>θJC</sub></b>	1.5	$^\circ C/W$

**Electrical Characteristics**  $T_c = 25^\circ\text{C}$ , unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Characteristics</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100	-	-	V
Gate-Body Leakage Current	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$T_J=25^\circ\text{C}$	$V_{DS} = 100V, V_{GS} = 0V$	-	-	1	$\mu A$
	$T_J=100^\circ\text{C}$		-	-	100	
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.4	1.8	2.4	V
Drain-Source on-Resistance <sup>2</sup>	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$	-	6.8	8	m $\Omega$
		$V_{GS} = 4.5V, I_D = 10A$	-	8.9	10.5	
Forward Transconductance	$g_{fs}$	$V_{DS} = 5V, I_D = 10A$	-	60	-	S
<b>Dynamic Characteristics</b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 50V, V_{GS} = 0V, f = 1\text{MHz}$	-	1890	-	$\mu F$
Output Capacitance	$C_{oss}$		-	352	-	
Reverse Transfer Capacitance	$C_{rss}$		-	9.7	-	
<b>Switching Characteristics</b>						
Gate Resistance	$R_G$	$V_{DS} = 0V, V_{GS} = 0V, f = 1\text{MHz}$	-	1.4	-	$\Omega$
Total Gate Charge	$Q_g$	$V_{GS} = 4.5V, V_{DD} = 50V, I_D = 20A$	-	15.2	-	nC
Total Gate Charge	$Q_g$	$V_{GS} = 10V, V_{DD} = 50V, I_D = 20A$	-	30.8	-	
Gate-Source Charge	$Q_{gs}$		-	5.8	-	
Gate-Drain Charge	$Q_{gd}$		-	3.9	-	
Turn-on Delay Time	$t_{d(on)}$	$V_{GS} = 10V, V_{DD} = 50V, R_G = 10\Omega, I_D = 20A$	-	6.7	-	nS
Rise Time	$t_r$		-	3.9	-	
Turn-off Delay Time	$t_{d(off)}$		-	19	-	
Fall Time	$t_f$		-	2.9	-	
<b>Drain-Source Body Diode Characteristics</b>						
Diode Forward Voltage <sup>2</sup>	$V_{SD}$	$I_S = 20A, V_{GS} = 0V$	-	-	1.2	V
Reverse Recovery Time	$t_{rr}$	$V_R = 50V, I_F = 20A, dI_F/dt = 500A/\mu s$	-	40	-	ns
Reverse Recovery Charge	$Q_{rr}$		-	160	-	nC

## Notes:

- The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- The EAS data shows Max. rating . The test condition is  $V_{DD}=25V, V_{GS}=10V, L=0.4\text{mH}, I_{AS}=34A$
- The power dissipation is limited by  $150^\circ\text{C}$  junction temperature

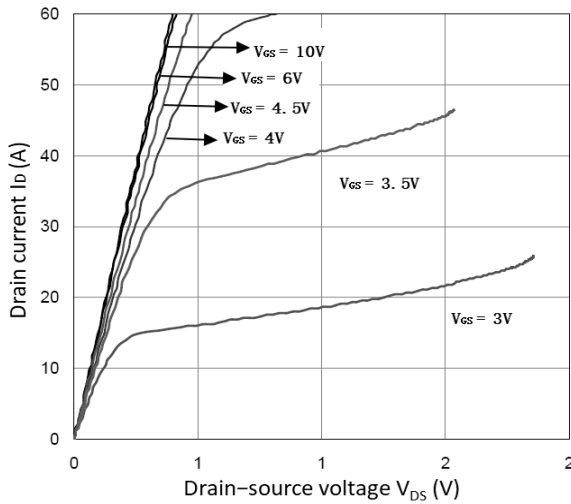


Figure 1. Output Characteristics

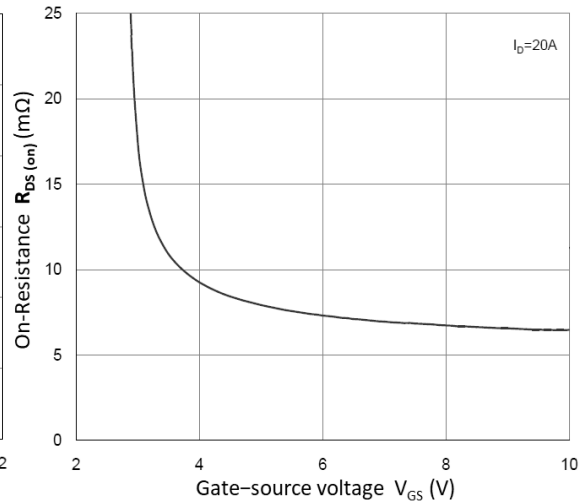


Figure 2.  $R_{DS(on)}$  vs.  $V_{GS}$

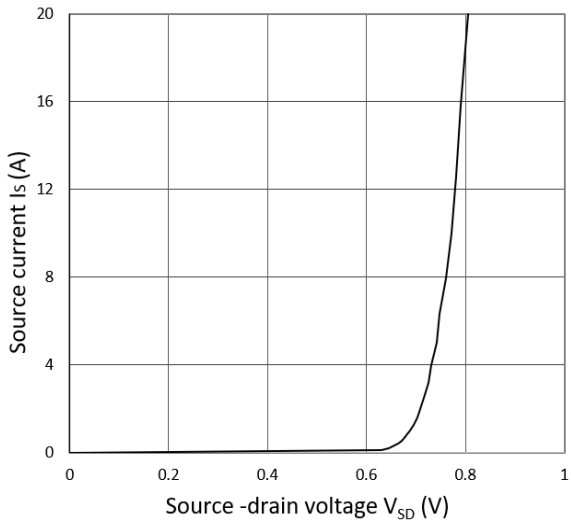


Figure 3. Forward Characteristics of Reverse

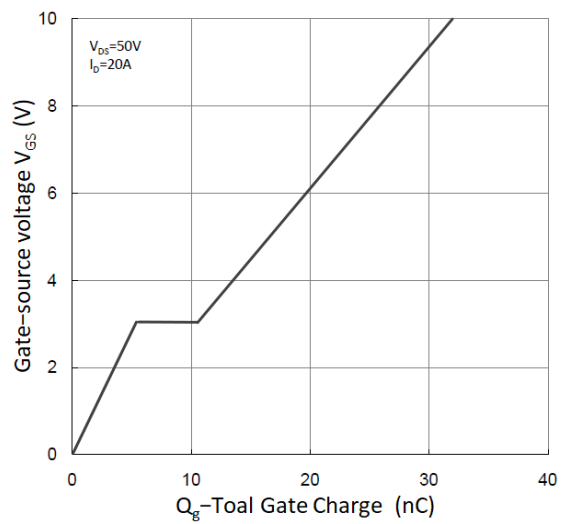


Figure 4. Gate Charge Characteristics

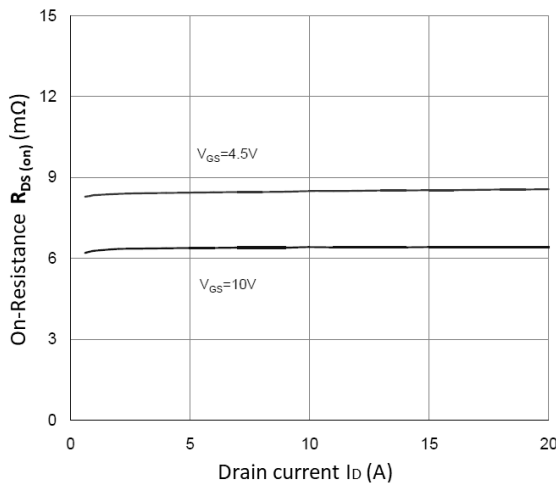


Figure 5.  $R_{DS(on)}$  vs.  $I_D$

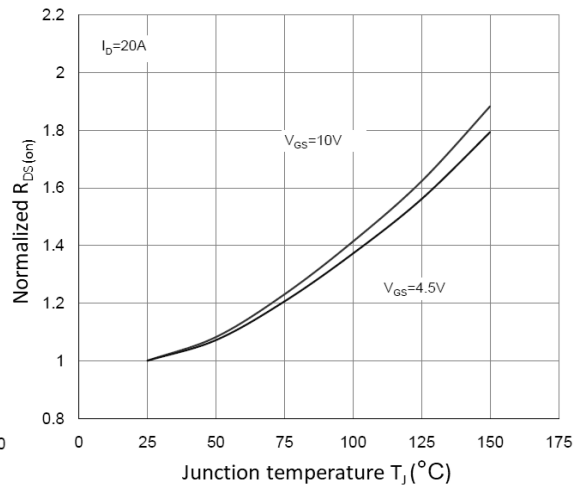


Figure 6. Normalized  $R_{DS(on)}$  vs.  $T_J$

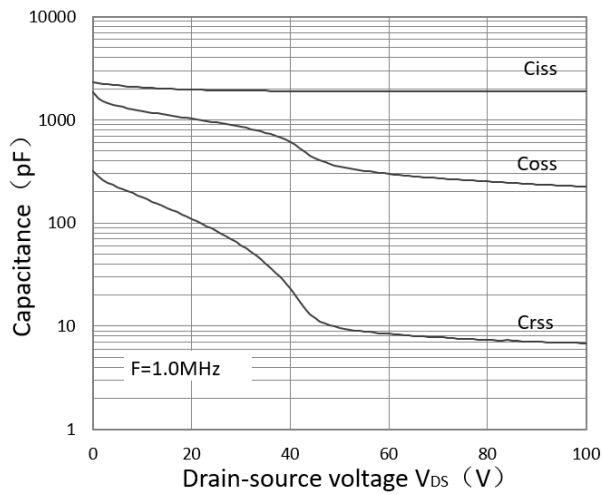


Figure 7. Capacitance Characteristics

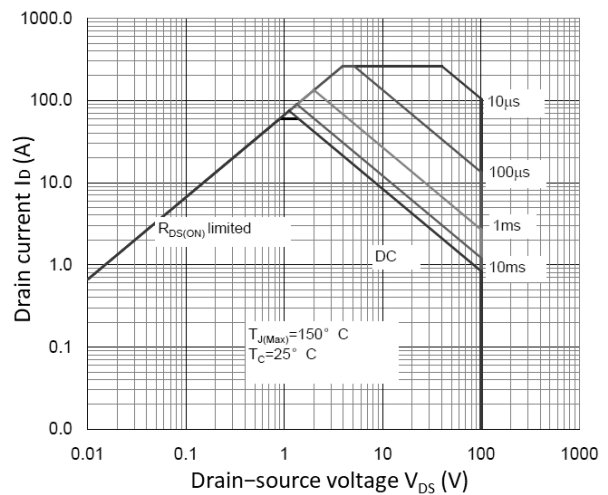


Figure 8. Safe Operating Area

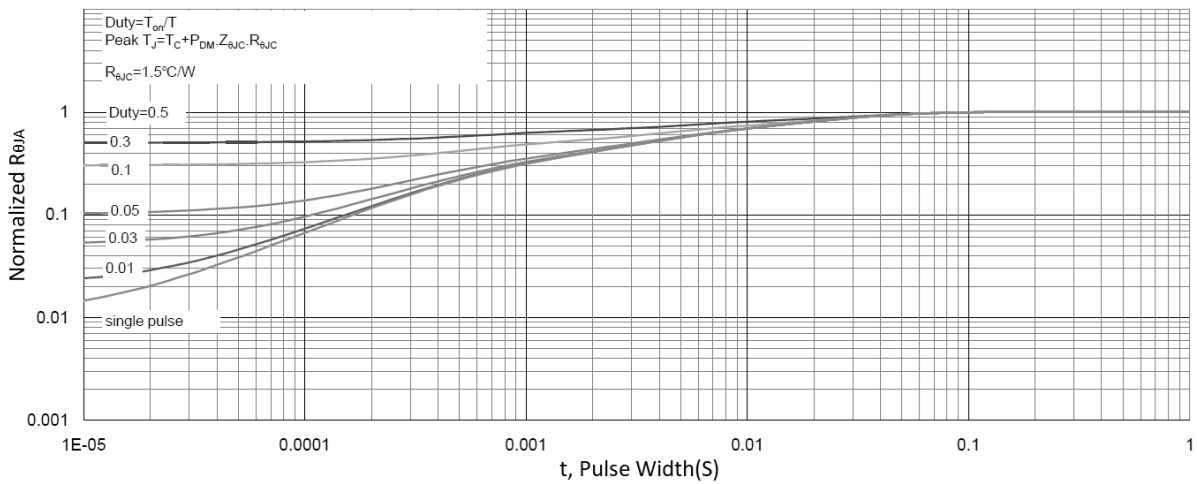


Figure 9. Normalized Maximum Transient Thermal Impedance

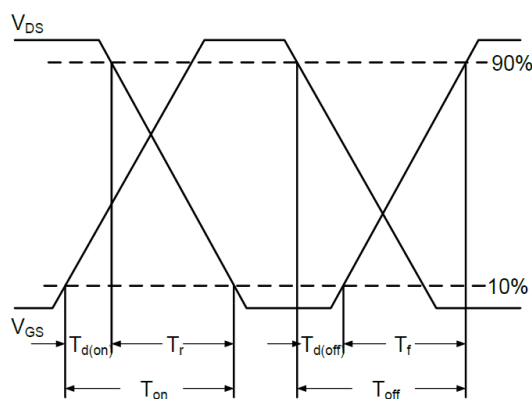


Figure 10. Switching Time Waveform

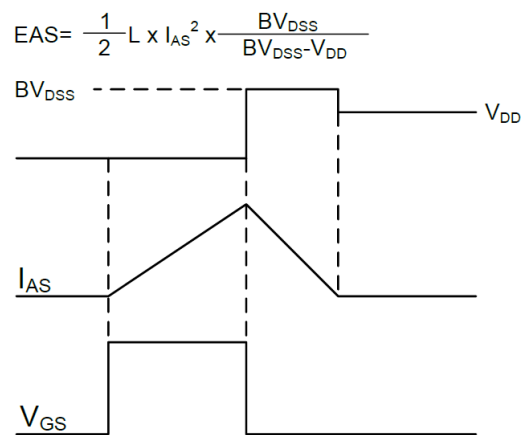
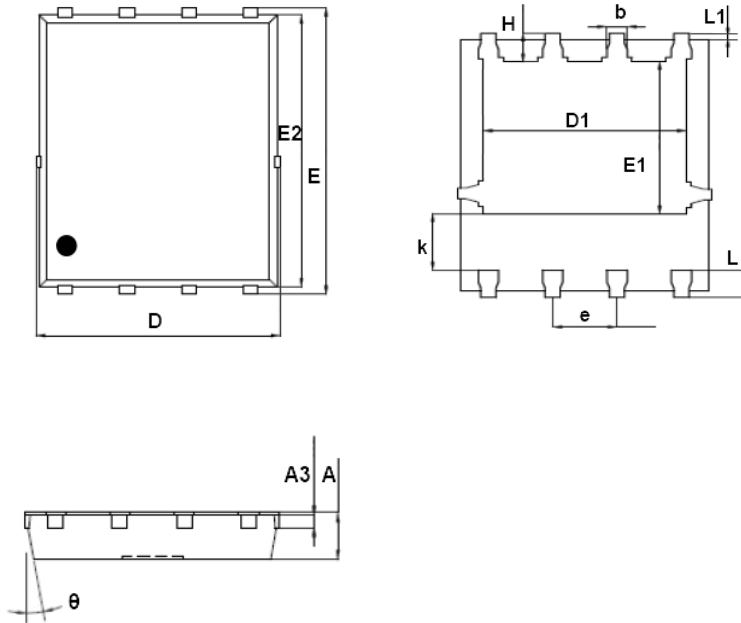


Figure 11. Unclamped Inductive Switching Waveform

## Mechanical Dimensions for PDFN5060-8L

## COMMON DIMENSIONS

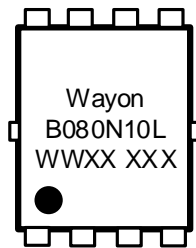


SYMBOL	MM	
	MIN	MAX
A	0.90	1.20
A3	0.15	0.35
D	4.80	5.40
E	5.90	6.35
D1	3.61	4.31
E1	3.30	3.92
E2	5.65	6.06
k	1.10	-
b	0.30	0.51
e	1.27BSC	
L	0.38	0.71
L1	0.05	0.36
H	0.38	0.61
$\theta$	0°	12°

## Ordering Information

Part	Package	Marking	Packing method
WMB080N10LG2	PDFN5060-8L	B080N10L	Tape and Reel

## Marking Information



B080N10L = Device code

WWXX XXX= Date code

## Contact Information

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