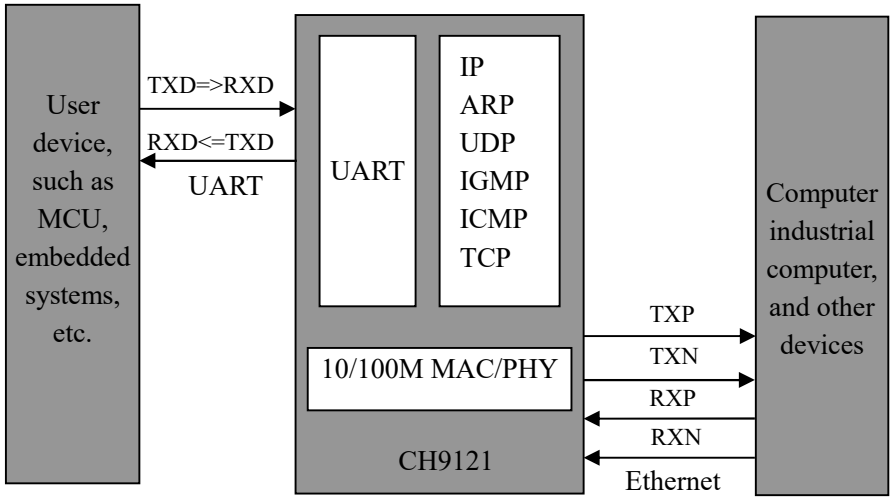
Network and UART Transparent Transmission Chip CH9121

Datasheet
Version: 2B
http://wch.cn

1. Overview

CH9121 is a chip realizing transparent transmission between network and UART. It integrates TCP/IP protocol stack, which can realize bidirectional transparent transmission between network data packets and serial data. It has 4 working modes: TCP CLIENT, TCP SERVER, UDP CLIENT and UDP SERVER. The serial baud rate can be up to 921600bps. It can be easily configured by upper computer software or serial commands, which is convenient and quick.

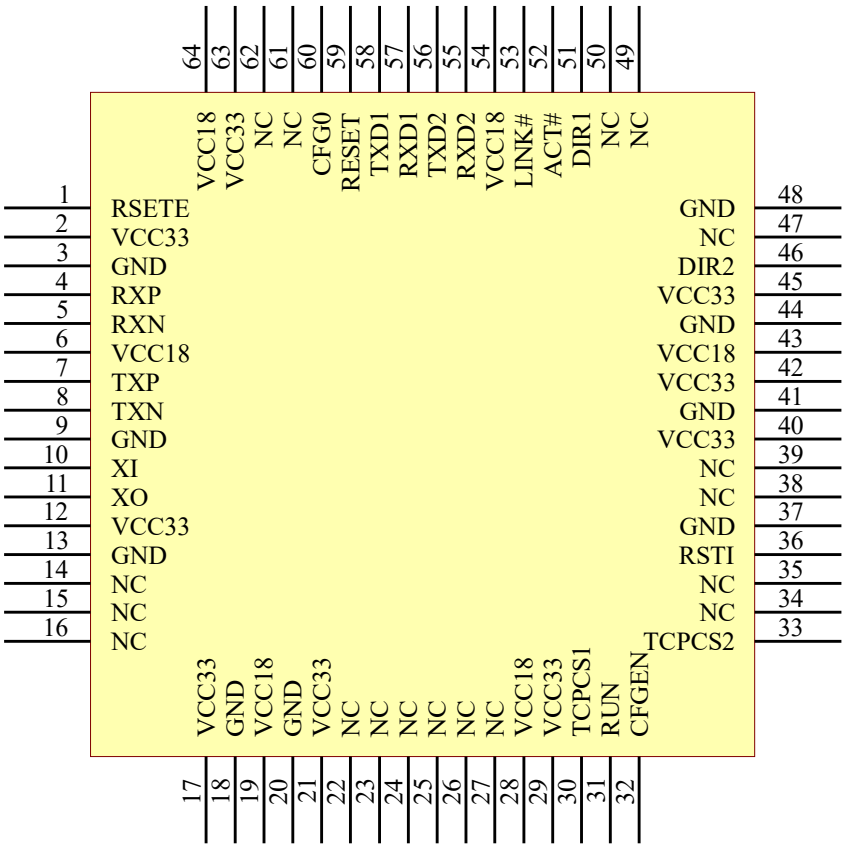
The figure below is a general application block diagram of CH9121.



2. Features

- Internal Ethernet MAC layer and PHY layer
- Realize bidirectional transparent transmission between serial data and network data
- Support 10/100M, full/half duplex self-adaption Ethernet interface, compatible with 802.3 protocol
- Support automatic MDI/MDIX line conversion
- Support DHCP automatic access to IP address, and DNS domain name access
- Set the chip working mode, port, IP and other network parameters through upper computer software and serial commands
- Support four working modes: TCP CLIENT, TCP SERVER, UDP CLIENT and UDP SERVER
- Support up to two independent UARTs, independent transparent transmission
- Serial baud rate supports 300bps ~ 921600bps
- Serial TTL level, compatible with 3.3V and 5V
- UART supports full-duplex and half-duplex serial communication, and RS485 transceiving automatic switch
- Support and provide virtual serial software
- Support KEEPALIVE mechanism

3. Package



Chip	Package	
	Name	Description
CH9121	LQFP64M	LQFP package; 64 pins; package body 10 x10mm

4. Pins

CH9121 Pin No.	Pin Name	Pin Type	Pin description
2, 12, 17, 21, 29, 40, 42, 45, 63	VCC33	Power	3.3V positive power input, require an external 0.1uF power decoupling capacitor
6, 19, 28, 43, 54, 64	VCC18	Power	1.8V positive power input, require an external 0.1uF power decoupling capacitor
3, 9, 13, 18, 20, 37, 41, 44, 48	GND	Power	Common ground
14, 15, 16, 22, 23, 24, 25, 26, 27, 34, 35, 38, 39, 47, 49, 50, 61, 62	NC	-	Reserved, suspended
1	RSETE	Input	Connected with an external 18K resistor to ground
4	RXP	Ethernet signal	Ethernet RXP signal
5	RXN	Ethernet	Ethernet RXN signal

		signal	
7	TXP	Ethernet signal	Ethernet TXP signal
8	TXN	Ethernet signal	Ethernet TXN signal
10	XI	Input	Input of the crystal oscillator, requires an external 30MHz crystal
11	XO	Output	Inverted output of crystal oscillator, requires an external 30MHz crystal
30	TCPCS1	Output	In TCP client mode, connection status indicator of port 1, active at low level
31	RUN	Output	CH9121 running status indicator pin, multiplexed as ISP upgrade pin
32	CFGEN	Input	Network configuration enable pin, detects when power-up, configuration disabled when at low level
33	TCPCS2	Output	In TCP client mode, connection status indicator of port 2, active at low level
36	RSTI	Input	External reset input, active at low level, built-in pull-up resistor
46	DIR2	Output	Used to control RS485 receiving/transmitting switch of UART2
51	DIR1	Output	Used to control RS485 receiving/transmitting switch of UART1
52	ACT#	Output	Ethernet connection communication indicator LED drive pin
53	LINK#	Output	PHY connection indicator LED, active low
55	RXD2	Input	Serial data input of UART2, built-in pull-up resistor (Off by default)
56	TXD2	Output	Serial data output of UART2 (Off by default)
57	RXD1	Input	Serial data input of UART1, built-in pull-up resistor (On by default)
58	TXD1	Output	Serial data output of UART1 (On by default)
59	RESET	Input	Restore factory settings, chip power-on detection, active at low level
60	CFG0	Input	UART configuration mode set pin, built in pull-up. If low level is detected, enter UART configuration mode. Exit the mode if high level is detected

5. Function

5.1. Function Description

CH9121 is a chip for transparent transmission between network and UART, and realizes bidirectional transparent transmission of serial data and network data. It supports 4 working modes (TCP CLEINT/SERVER, UDP CLIENT/SERVER), and the serial baud rate supported ranges from 300bps to 921600bps. Before use, the network parameters and UART parameters of the chip shall be configured by upper computer software NetModuleConfig.exe or serial commands. After the configuration is completed, CH9121 will save the configuration parameters to the internal storage space. And after the chip is reset, CH9121 will work according to the saved configuration value.

The basic parameters of CH9121 include: name, MAC address display, dynamic access IP address setting, manual IP address setting (including CH9121 IP address, subnet mask, default gateway), and UART negotiation configuration.

The name is mainly for the convenience of CH9121 module management within the LAN, with the length of not more than 20 bytes. The MAC address field shows the MAC address of the currently selected

module. There are two ways for CH9121 to set network parameters. 1) DHCP, that is, it automatically obtains network parameters from the gateway device with DHCP SERVER function; 2) manual setting. UART negotiation configuration function is to enter serial configuration mode by handshaking through the UART, which is disabled by default.

CH9121 port parameters include: network mode, local port, target IP/domain name, destination port, serial baud rate/data bit/stop bit/parity check bit, network cable disconnection processing, RX packet length, RX packet timeout interval, network connection operation.

The network mode (TCP SERVER/CLIENT, UDP SERVER/CLIENT), destination IP address, and local/destination port are the basic parameters of network communication. The destination IP address can also be accessed by domain name. The serial baud rate ranges from 300bps to 921600bps (the baud rate error of the serial port transmitting signal is less than 0.3%, and the allowable baud rate error of the serial port receiving signal is not less than 2%). It supports 5/6/7/8 data bits, 1/2 stop bits, odd/even/no parity check, blank 0, and mark 1 check mode. The network cable disconnection processing means that when the network cable is disconnected, CH9121 actively closes the connection or does not take any action. The length range of RX packet is 1-1024, which means that when the length of CH9121 UART receiving data reaches the set length, CH9121 will immediately packet the serial data and send it out via network. The timeout time setting range is 0-200, and the timeout unit is about 5ms. For example, when the timeout is 1, the data length of the serial port receiving buffer does not reach the length of the RX packet, and the serial port does not receive a new one in more than 5ms, the serial port timeout will occur. After the serial port timeout occurs, CH9121 will send the data received by the serial port over the network. When the timeout time is set to 0, the internal hardware timeout mechanism will be enabled (no new data is received after 4 data times), which is suitable for occasions where real-time requirements are high and large quantities of data are sent and received. Clear serial port buffer setting refers to how the data received by the serial port is processed before the network connection is established, the data is cleared (discarded) or retained after TCP connection.

5.2. Default Configuration

When CH9121 leaves factory, port 2 is closed and port 1 works in TCP CLIENT mode by default. The default parameters related to the network are as follows:

（1） Device IP: 192.168.1.200
（2） Subnet mask: 255.255.255.0
（3） Default gateway: 192.168.1.1
（4） Module port: 2000
（5） Destination IP: 192.168.1.100
（6） Destination port: 1000
（7） Number of reconnection: unlimited

UART related default parameters are:

（1） Baud rate: 9600
（2） Timeout: 0
（3） Data bit: 8. Stop bit: 1. Parity check bit: No
（4） Clear UART buffer: Never

6. Parameters

6.1. Absolute Maximum Value

Critical value or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged.

Name	Parameter description		Min.	Max.	Unit
TA	Ambient temperature during operation	VCC33=3.3V VCC18=1.8V	-40	85	℃

TS	Ambient temperature during storage	-55	125	℃
VCC33	Supply voltage (VCC33 connects to power, GND to ground)	-0.4	4.2	V
VCC18	Supply voltage (VCC18 connects to power, GND to ground)	-0.4	2.3	V
VIO	Voltage on input or output pins	-0.4	VCC33+0.4	V
VIO5	Voltage on input or output pins that support 5V withstand voltage	-0.4	5.4	V

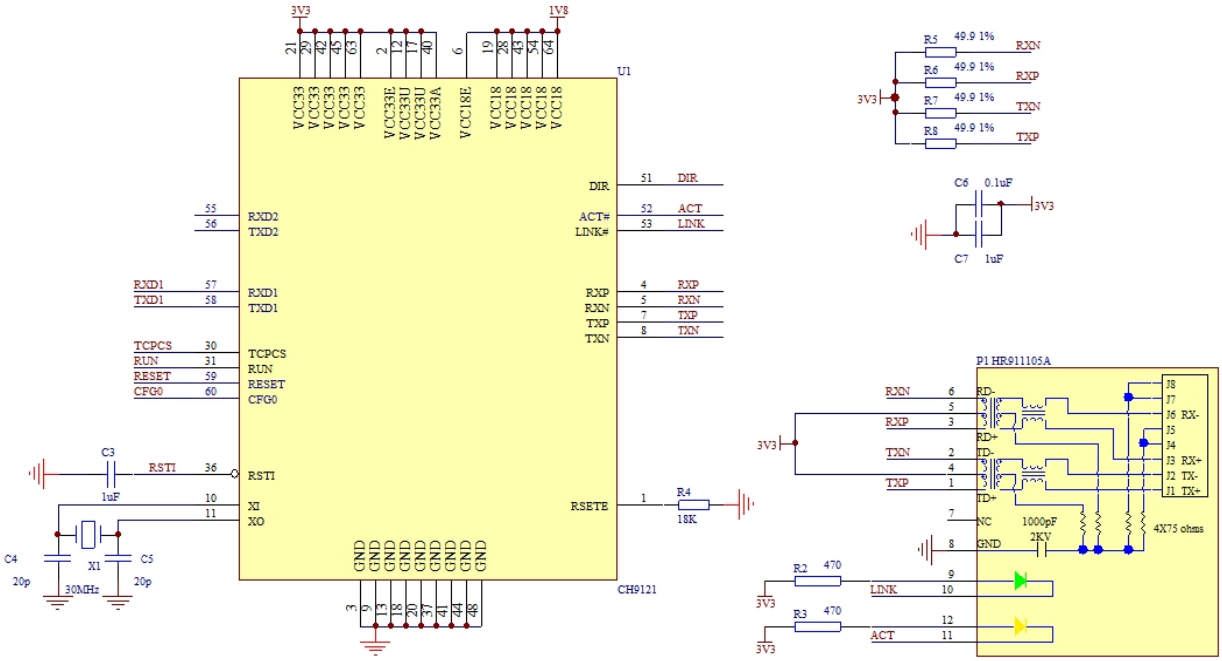
6.2. Electrical Parameters

Test Conditions: TA=25℃, VCC33=3.3V, VCC18=1.8V

Name	Parameter description		Min.	Typ.	Max.	Unit
VCCxx	Supply voltage	VCC33	2.7	3.3	3.6	V
		VCC18	1.65	1.8	1.95	
ICC	Total supply current during operation	VCC33=3.3V		160	190	mA
VIL	Low level input voltage		-0.4		0.7	V
VIH	High level input voltage		2.0		VCC33+0.4	V
VOL	Low level output voltage (4mA draw current)				0.4	V
VOH	High level output voltage (4mA output current)		VCC33-0.4			V
IUP	Input current at the input terminal with built-in pull-up resistor		20	40	100	uA
IDN	Input current at the input terminal with built-in pull-down resistor		-20	-40	-100	uA
VR	Voltage threshold when power-on reset		1.4	1.5	2.5	V

7. Applications

7.1 Hardware Circuit Design



Note: Due to space limitations, the circuit of the power supply and decoupling capacitors near the 3.3V and 1.8V pins is omitted in the figure, which must be added when designing the circuit. The detailed circuit reference file: CH9121PCB (please download in our official website).

U1 is the main control chip CH9121. TXD1 and RXD1 are compatible with 3.3V and 5V level, and the RS485 control pin DIR can be suspended if not used.

P1 is RJ45 port, with built-in network transformer, used to connect network equipments such as switches and router. It contains two pairs of Ethernet differential signals.

When actually making a PCB, R5-R8, C6, and C7 should be as close as possible to the 5th pin of P1. The 0.1 uF decoupling capacitors for 3.3V and 1.8V pins are omitted in the figure. TXOP (RXIP) and TXON. (RXIN) are differential signals. When wiring, they should be wired close to parallel, and try to provide ground wire or copper coating on both sides to reduce external interference. The length of relevant signals of crystals XI and XO should be shortened as much as possible. In order to reduce the interference of high-frequency clock for the outside, the baselines should be surrounded or copper should be clad around relevant components.