CH32V103 Datasheet

V1.0

Overview

The 32-bit RISC processor RISC-V3A is based on the RISC-V open source command set design, and its system architecture achieves the best balance of low cost, low power consumption and functional applications of the hardware platform.

With this processor as the core, the CH32V1 series of general microcontrollers is equipped with abundant peripheral interfaces and functional modules, including clock security mechanism, multi-level power management, general DMA controller, multi-channel 12-bit ADC conversion module, multi-channel touch key capacitance detector (TKey), advanced and general timers, USB2.0 host controller and device controller and multichannel I2C/USART/SPI interfaces, etc. The microcontroller is equipped with a complete software and hardware platform and debugging interface tools to meet various needs in the industrial, medical, consumer and other markets.

Features

- **Core:**
  - Support RV32IMAC command set combination, hardware multiplication and division
  - Fast programmable interrupt controller + hardware site save and recovery
  - Static branch prediction and conflict handling mechanism
  - Low power two-stage assembly line
  - Up to 80MHz system frequency
- **Memory:**
  - 20KB volatile data storage area, SRAM
  - 64KB user application storage area, CodeFlash
  - 3.75KB system storage area, BootLoader
  - 128KB system non-volatile configuration information memory area
  - 128B user-defined information storage area
- **Power Management and Low Power:**
  - Power supply range: 2.7V～5.5V, GPIO synchronous power supply voltage
  - Multiple low power consumption modes: sleep/stop/standby
  - V_{BAT} power independently supplies power to RTC and backup registers
- **System clock and reset**
  - Built-in factory-calibrated 8MHz RC oscillator
  - Built-in 40KHz RC oscillator
  - Built-in PLL, optional CPU clock up to 80MHz
  - Externally support 4MHz～16MHz high-speed oscillator
  - Externally support 32.768KHz low-speed oscillator
  - Power-on/power-down reset (POR/PDR), programmable voltage detector (PVD)
- **Real-time clock (RTC):** 32-bit independent timer
- **General-purpose DMA controller**
  - Provide 7 channels
  - Support peripherals and memories
  - Support ring buffer area management
  - Support peripherals: TIM/ADC/USART/I2C/SPI
- **12-bit ADC**
  - Conversion range: 0～V_{DDA}. The conversion is completed in1us at the fastest
  - 16 external signal channels + 2 internal signal channels
  - Temperature sensor on chip
- **16-channel Touch-Key channel detection**
- **7 timers**
  - One 16-bit advanced timer, including general-purpose timer function, and provided with dead zone control and emergency brake, provide PWM for motor control
  - Three16-bit general-purpose timers, provide up to 4 channels for input capture/output comparison/PWM/pulse counting and incremental encoder input
  - 2 watchdog timers (independent and window type)
  - System time timer: 64-bit self-increment counter
- **8 Standard Communication interfaces:**
  - USB2.0 host/ device interface (full speed and low speed)
  - 2 I2Cs (support SMBus/PMBus)

-3 USARTs (support ISO7816 interface, LIN, IrDA interfaces and modem control)
-2 SPIs (support Master and Slave modes)

- **Fast GPIOs**

-Up to 51 I/Os, and can be mapped to 16 external interrupts

- **Security features:** CRC calculation unit, 96-bit chip unique ID
- **Debug mode:** Serial 2-wire debug interface
- **Package**

- LQFP64M (LQFP64-10*10)
- LQFP48 (LQFP48-7*7)
- QFN48X7 (QFN48-7*7)

Chapter 1 Specification Information

CH32V1 series MCU products use RISC-V3A processor and architecture, and support RV32IMAC open source commands. The highest operating frequency is 80MHz, a built-in high-speed memory is provided, and prefetching method is adopted to improve the command access speed. Multiple buses in the system structure work synchronously, providing abundant peripheral functions and enhanced I/O ports. This series of products have built-in functions such as RTC, clock security mechanism, one 12-bit ADC conversion module, multiple sets of timers, 16-channel touch key capacitance detection (TKey), and also include standard communication interfaces: 2 I2C interfaces, 2 SPIs Interface, 3 USART interfaces and 1 USB2.0 full-speed host/device interface (full/low-speed communication).

The supply voltage range of this series of products is 2.7V～5.5V, and the operating temperature range is -40℃～85℃ industrial grade. They support a variety of power-saving operating modes to meet the low-power application requirements. The products in this series are different in terms of resource allocation, number of peripherals, peripheral functions, etc. You can choose according to your needs. Several packages forms are provided: LQFP64M/LQFP48/QFN48X7. It can be widely used in: motor drive and application control, medical and handheld devices, PC game peripherals and GPS platforms, programmable controllers, inverters, printers, scanners, alarm systems, video intercom, heating, ventilation and air conditioning systems, etc.

1.1 Model Comparison

Table 1-1 CH32V103x Product Resource Allocation

Model / Difference		CH32V103 C6T6	CH32V103 C8T6	CH32V103 C8U6	CH32V103 R8T6
Number of chip pins		48	48	48	64
Flash memory (byte)		32K	64K	64K	64K
SRAM (byte)		10K	20K	20K	20K
Number of GPIOs		37	37	37	51
Timer	General-purpose	2	3	3	3
	Advanced	1	1	1	1
	Watchdog (WDT)	2	2	2	2
	System clock	1	1	1	1
ADC/TKey (Number of channels)		10	10	10	16
Communication Interface	SPI	1	2	2	2
	I2C	1	2	2	2
	USART	2	3	3	3
	USBHD 2.0FS	1	1	1	1
CPU main frequency		Typical: 72MHz			
Operating voltage		2.7V～5.5V			
Operating temperature		Industrial grade -40℃~85℃			
Package		LQFP48		QFN48X7	LQFP64M(10*10)

1.2 System Framework

CH32V1 series products are general-purpose microcontrollers designed based on RISC-V3A processor. The

core, arbitration unit, DMA module and SRAM memory, etc. of the architecture interact through multiple sets of buses. The 2-level assembly line processing is adopted for the core, and is equipped with static branch prediction and command prefetching mechanisms to achieve the best performance ratio of the system with low power consumption, low cost, and high-speed operation. The controller is equipped with a general DMA controller to reduce the burden on the CPU and improve efficiency. The clock tree hierarchical management reduces the total operating power consumption of peripherals. At the same time, it also has a data protection mechanism and a clock security system protection mechanism to increase the system stability.

The figure below is the internal framework diagram.

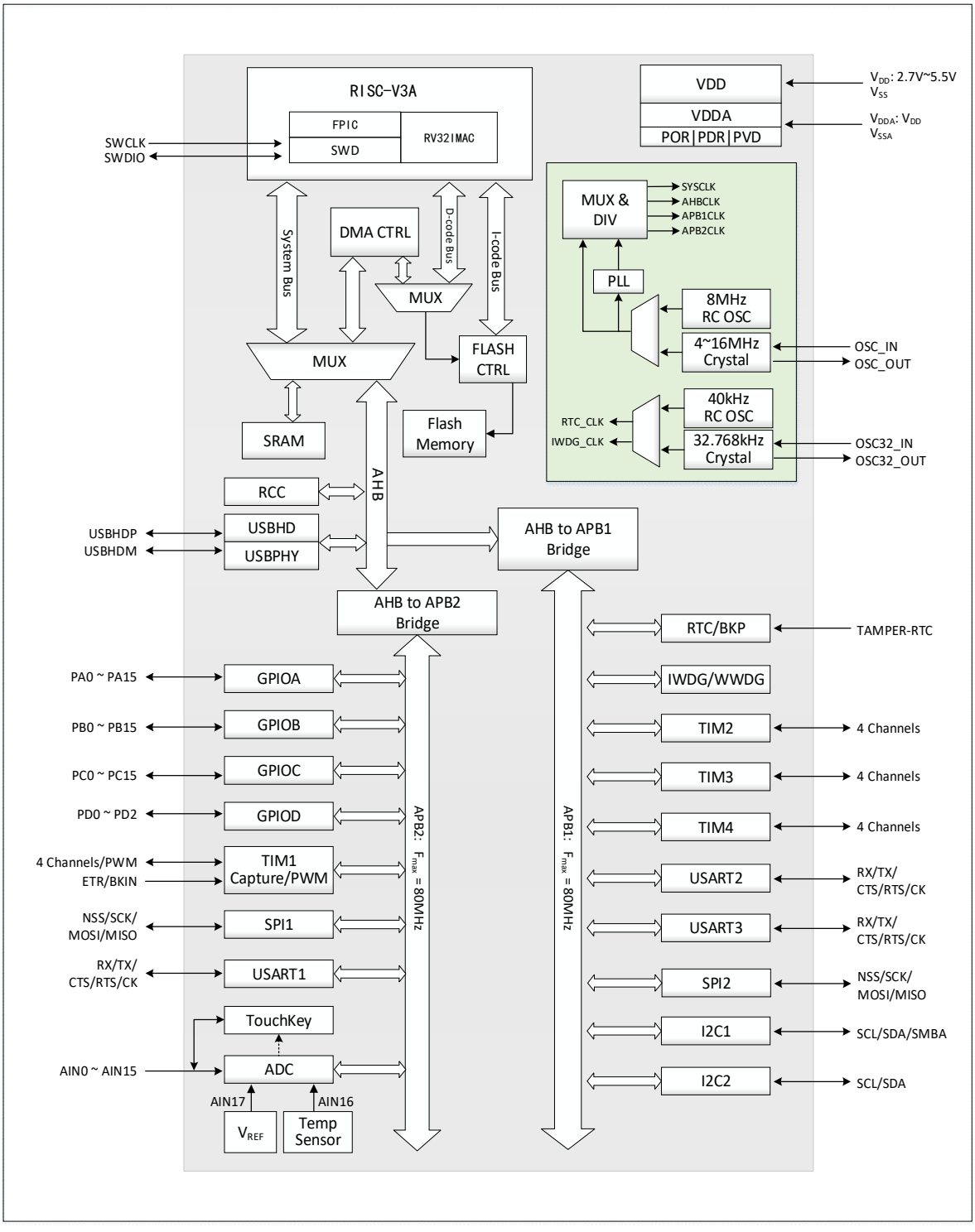

Figure 1-1 System Block Diagram

1.3 Memory Mapping Table

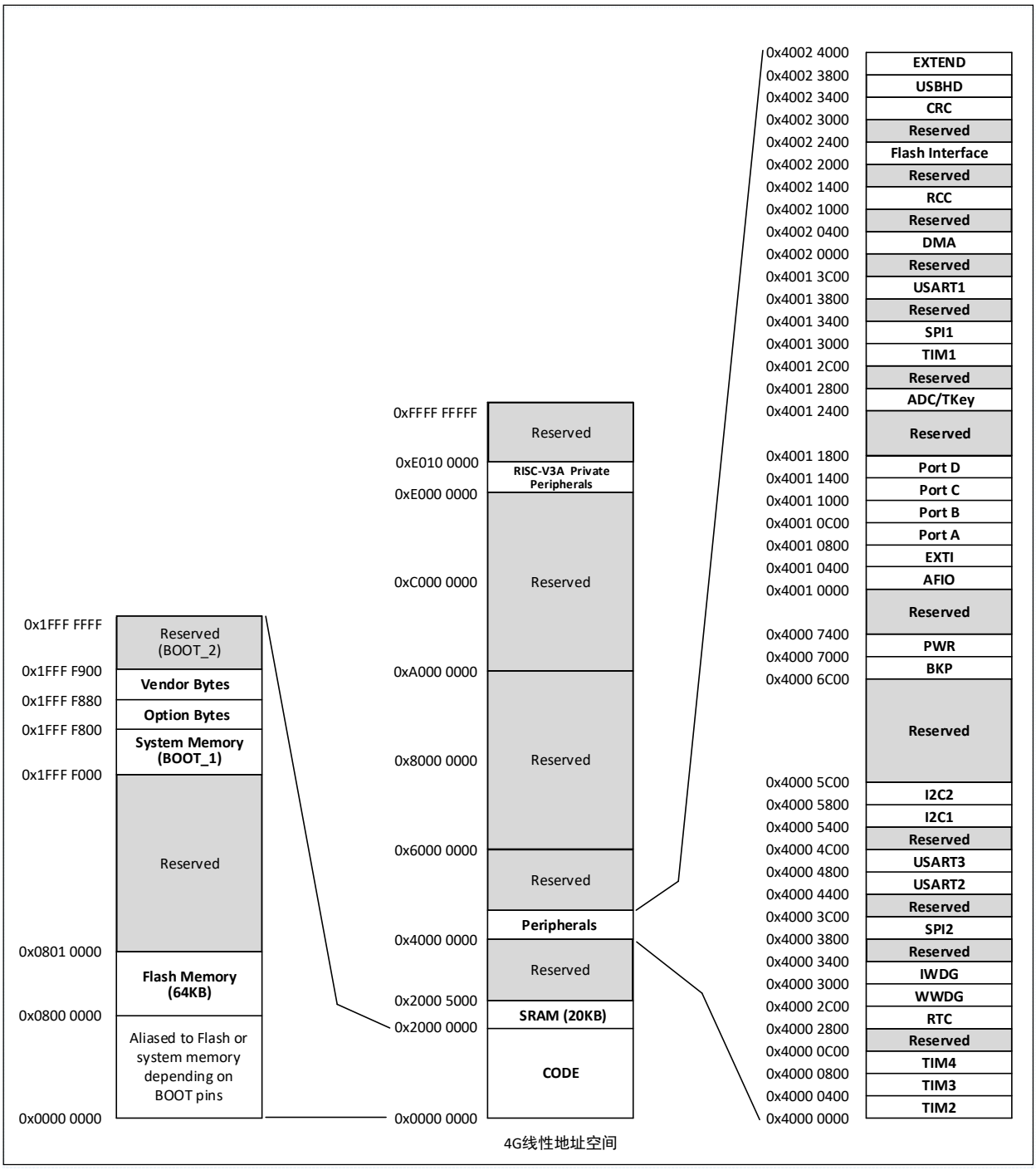

Figure 1-2 Memory Address Mapping

1.4 Clock Tree

The system provides 4 sets of clock sources: internal high frequency RC oscillator (HSI), internal low frequency RC oscillator (LSI), external high frequency oscillator or clock signal (HSE), external low frequency oscillator or clock signal (LSE). Among them, the system bus clock (SYSCLK) comes from a high-frequency clock source (HSI/HSE) or a higher clock generated by the PLL multiplication. The AHB domain, APB1 domain, and APB2 domain are obtained by the system clock or the frequency division by the previous-level corresponding prescaler.

The low-frequency clock source provides a clock reference for the RTC and independent watchdog.

The PLL frequency multiplication clock directly provides the working clock reference 48MHz of the USBHD module through the frequency divider.

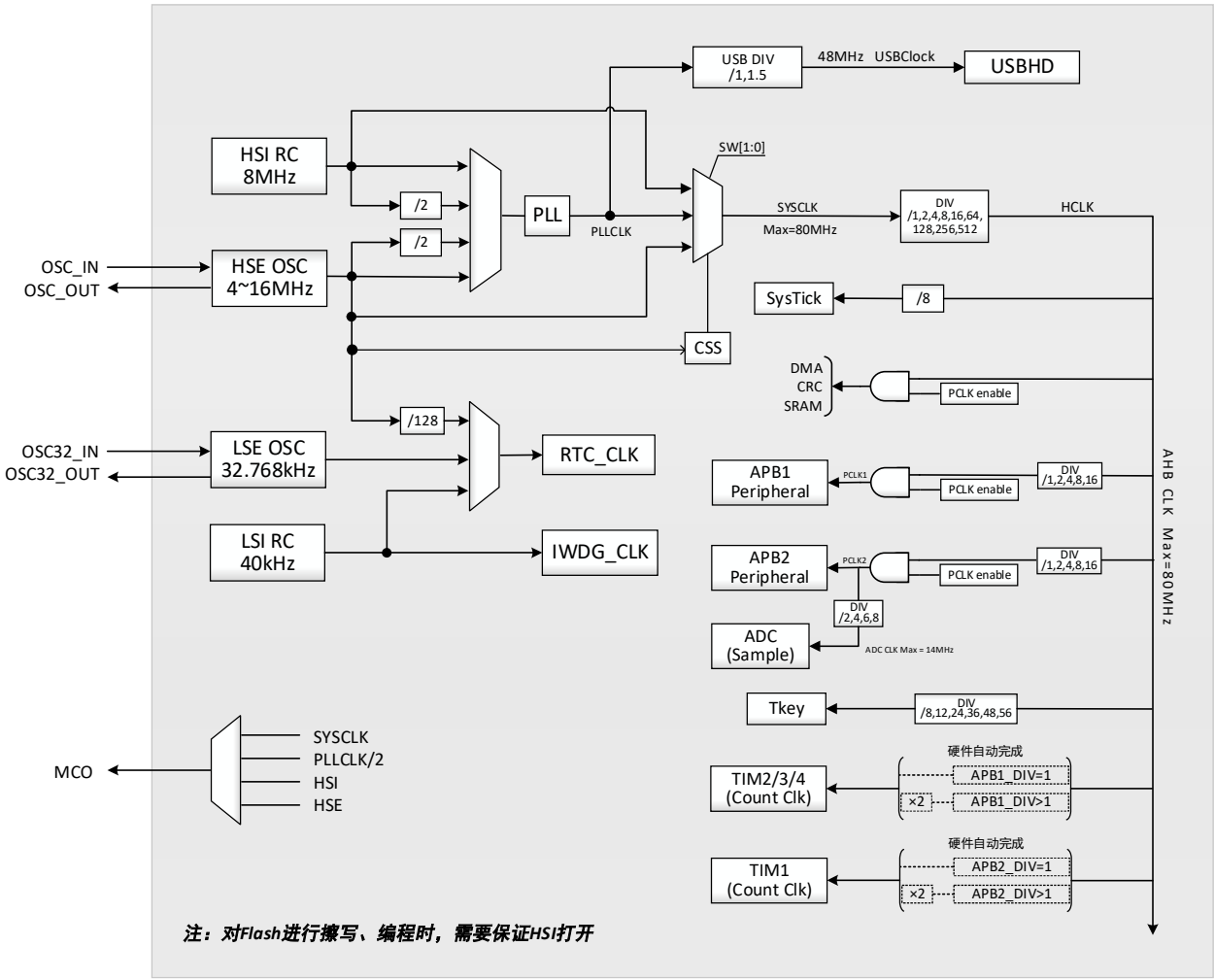

Figure 1-3 Clock Tree Block Diagram

Note:

When the USB function is used, the PLL must be used at the same time, and the CPU frequency must be 48MHz or 72MHz.

When the ADC sampling time is 1us, APB2 must be set to 14MHz, 28MHz or 56MHz.

When the system wakes up from sleep, the system will automatically switch to HSI as the main frequency.

When erasing, writing and programming Flash, you must ensure that HSI is turned on.

1.5 Function Overview

1.5.1 RISC-V3A Processor

RISC-V3A is a 32-bit embedded processor with internal modular management and supports the IMAC subset of the RISC-V open source command set. It includes Fast Programmable Interrupt Controller (FPIC), provides 4 vector programmable fast interrupt channels and 44 priority configurable ordinary interrupts, and realizes the shortest cycle response of interrupts by means of hardware on-site storage and restoration. It includes 2-wire serial debugging interface, supports user online upgrading and debugging. It includes multiple sets of buses

connected to the external unit modules of processor to realize the interaction between external function modules and the core.

- RV32IMAC command set, small-end data mode
- Low-power two-level assembly line
- Support machine and user privilege mode
- Fast Programmable Interrupt Controller (FPIC), Tail-Chaining interrupt processing, 2-level hardware push to stack
- Serial 2-wire debugging interface
- Branch prediction, efficient jump, conflict detection mechanism

The processor based on this design can be flexibly applied to microcontroller designs in different scenarios, such as small-area, low-power-consumption embedded scenarios, and high-performance application operating system scenarios with its features such as minimal instruction set, multiple working modes, and modular customization extension.

The CH32V1 series controller adopts the RISC-V3A core, is equipped with a complete software and hardware platform and tools, and supports online download, debugging, and tracking of application codes.

1.5.2 On-chip Memory and Boot Mode

The built-in 20K bytes SRAM area for saving the data.

The built-in 64K bytes program flash memory storage area (CodeFlash) for saving the user's application program.

The built-in 3.75K bytes system storage area (BootLoader) for saving the system guidance programs (manufacturer's solidified boot loading program).

In addition, 128 bytes are used for saving the manufacturer's configuration word and 128 bytes are used for saving the selection words by the user.

During the startup, one of three bootstrap modes can be selected through the boot pins (BOOT0 and BOOT1):

- Boot from the program flash memory
- Boot from the system memory
- Boot from the internal SRAM

The boot loading program is saved in the system storage area and the contents of the program flash memory storage area can be re-programmed through the USART1 and USB interfaces.

1.5.3 Power Supply Scheme

- V_{DD} = 2.7～5.5V; the V_{DD} pin supplies power to the I/O pin, RC oscillator, reset module and internal voltage regulator.
- V_{DDA} = 2.7～5.5V: it supplies power to the simulation part of ADC, temperature sensor and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}.
- V_{BAT} = 1.8～5.5V: When the V_{DD} is removed or does not work, V_{BAT} will separately supply power to RTC, external 32 KHz oscillator and backup register.

1.5.4 Power Supply Monitor

This product internally integrates a power-on reset (POR)/power-down reset (PDR) circuit, which is always in the working condition to ensure that the system works when the power supply exceeds 2.7V; when V_{DD} is

lower than the set threshold ($V_{POR/PDR}$)), place the device in the reset state, and an external reset circuit does not need to be used.

In addition, there is a programmable voltage detector (PVD), which needs to be switched on by software to compare the voltage of V_{DD}/V_{DDA} power supply and the set threshold V_{PVD}. Open the corresponding edge interrupt of PVD. When the V_{DD} is reduced to PVD threshold or increased to PVD threshold, the interrupt notice will be received. Refer to Table 3-4 for the values on $V_{POR/PDR}$ and V_{PVD}.

1.5.5 Voltage Regulator

After reset, the regulator will be automatically switched on. There are three operation modes according to the application method.

- Start mode: The stable core power supply is provided through the normal operation
- Low power mode: After CPU enters the stop mode, you can select to operate the regulator at low power consumption
- Switching-off mode: When CPU enters the standby mode, the regulator will be automatically switched to the mode, and the voltage regulator will output as high resistance status. Supply of core circuit is disconnected, the voltage regulator is in zero consumption status.

The voltage regulator is always at the start mode after reset, and will be switched off and at the switching-off mode in the standby mode. At this moment, high resistance is outputted.

1.5.6 Low Power Mode

The series products support three low power modes and can reach the optimum balance under the conditions of low power, short start time and multiple wake-up events.

- Sleep Mode

WFI/WFE command is implemented. In the sleep mode, only the CPU clock stops, but the power supply of all peripheral clocks is normal and the peripherals are at the working state. The mode is the shallowest power consumption mode, but can reach the fastest wake-up.

Exit conditions: Any interrupt or wake-up event.

- Stop mode

Clear the PDDS bit, set the SLEEPDEEP bit, select to clear/ set LPDS bit and execute the WFI/WFE command to enter. In the stop mode, FLASH will enter the low power consumption mode, and LPDS bit decides whether the power supply of core part will be shut down, and the RC oscillator and HSE crystal oscillator of PLL and HSI will be shut down. In the stop mode, the power consumption can reach the lowest when the contents of SRAM and register are maintained not to be lost.

Exit conditions: Any external interrupt / event (EXTI signal), external reset signal on NRST, IWDG reset and a rising edge on WKUP pin; whereof EXTI signals include one of 16 external I / O ports, PVD output, RTC alarm clock or USB wake-up signal.

- Standby mode

Set the PDDS and SLEEPDEEP bits and execute WFI / WFE command to enter. The power supply of the core part is turned off; the RC oscillator and HSE crystal oscillator of PLL and HSI are also turned off; the minimum power consumption can be achieved in this mode, but the system will reset after wake-up.

Exit conditions: Any external interrupt / event (EXTI signal), external reset signal on NRST, IWDG reset and a

rising edge on WKUP pin; whereof EXTI signals include one of 16 external I / O ports, PVD output, RTC alarm clock or USB wake-up signal.

1.5.7 Cyclic Redundancy Check (CRC) Calculation Unit

CRC (cyclic redundancy check) calculation unit uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. In many applications, CRC based technology is used to verify the consistency of data transmission or storage. Within the scope of EN/ IEC 60335-1 standard, a method of detecting flash memory error is provided. The CRC calculation unit can be used to calculate software signature real-timely and it shall be compared with the signature generated when linking and generating the software.

1.5.8 Fast Programmable Interrupt Controller (FPIC)

The product has built-in fast programmable interrupt controller (FPIC), which supports up to 255 interrupt vectors. Ch32v1 controller provides 5 core private interrupts and 44 peripheral interrupt management, and other interrupt sources are reserved. FPIC registers can be accessed in both user and machine privilege modes.

- 44 + 3 separate maskable interrupts
- Providing a non-maskable interrupt NMI
- 16-level priority programming, modified dynamically.
- For level-2 nesting interrupt entry and exit and hardware automatic stacking and recovery; no instruction overhead is required
- 4-channel programmable fast interrupt channel; custom interrupt vector address
- Supporting interrupt tail link function
- Providing the prompt response of non-maskable interrupt

The module provides flexible interrupt management with minimal interrupt delay.

1.5.9 External Interrupt / Event Controller (EXTI)

The external interrupt / event controller contains 20 edge detectors for generating interrupt / event requests. Each interrupt line can be configured independently with its trigger event (rising edge or falling edge or double edges), and can be masked independently. The register can be hung to maintain all interrupt request states. EXTI can detect that the pulse width is less than the internal APB2 clock cycle. Up to 51 general-purpose I/Os can be selectively connected to 16 external interrupt lines.

1.5.10 General-purpose DMA Controller

Flexible general-purpose DMA can manage the high-speed data transmission from memory to memory, peripheral to memory and memory to peripheral, providing 7 channels and supporting ring buffer area management. Each channel has special hardware DMA request logic, which supports the access request of one or more peripheral devices to the memory and data transmission from memory to memory. The access priority, transmission length, source address and destination address of transmission can be configured.

The main peripherals used in DMA include: General-purpose / advanced control timers TIM, ADC, USART, I2C, SPI.

1.5.11 Clock and Startup

The system clock source HSI is on by default. After no clock is configured or reset, the internal 8MHz RC oscillator will be used as the default CPU clock, and then the external 4-16MHz clock or PLL clock can be

selected. After the clock safety mode is switched on, if HSE is used as the system clock (directly or indirectly), the system clock will be automatically switched to the internal RC oscillator and HSE and PLL will be automatically turned off when the system detects the external clock failure; for the low power consumption mode of switching off the clock, the system will also automatically switch to the internal RC oscillator after wake-up. If the clock interrupt is enabled, the software can receive corresponding interrupt.

Multiple prescalers are used to configure AHB bus clock, high-speed APB2 and low-speed APB1 area bus clock. Refer to the clock tree block diagram of Figure 1-2.

1.5.12 RTC (Real-time Clock) and Backup Register

The RTC and backup register are in the backup power supply area inside the product. When the V_{DD} is valid, the power will be supplied by the V_{DD}. Otherwise, the V_{BAT} pin will be automatically switched internally to supply the power.

RTC real-time clock is a group of 32-bit programmable counters. The time base supports 20-bit prescaler, which is used for the measurement in the long period. The clock reference source is high-speed external clock 128 frequency division (HSE/128), 32.768KHz oscillator (LSE) of external crystal or internal low-power-consumption RC oscillator (LSI). The LSE also has a backup power supply area. Therefore, when LSE is selected as RTC time base, the setting and time of RTC can remain unchanged after the system is reset or woken up from the standby mode.

The backup register includes ten 16-bit registers, which can be used to store 20 bytes of user application data. The data can be maintained and will not be reset after the standby wake-up, or when the system is reset or the power is reset. When the intrusion detection function is switched on, once the intrusion detection signal is valid, all contents in the backup register can be cleared.

1.5.13 ADC (Analog to Digital Converter) and Touch Button Capacitance Detection (Tkey)

A 12-bit analog-to-digital converter (ADC) is embedded in the product, providing up to 16 external channels and 2 internal channels for sampling. For the programmable channel sampling time, single, continuous, scanning or intermittent modes conversion can be achieved. The analog watchdog function that allows very accurate monitoring of one or more selected channels is provided for monitoring the channel signal voltage. Supporting external event trigger conversion; the trigger sources include internal signal and external pin of on-chip timer (EXTI line 11). It supports DMA operation.

The ADC internal channel sampling includes one-circuit built-in temperature sensor sampling and one-circuit internal reference power sampling. The temperature sensor generates a voltage that varies linearly with temperature, and the power supply range is $3.0V < V_{DDA} < 5.5V$. The temperature sensor is internally connected to the ADC_ IN16 input channel, used to convert the output of the sensor to a digital value.

The touch key capacitance detection function multiplexes the external channel of ADC to provide up to 16 circuits of detection. The application program judges the status of touch key based on the change of digital value.

1.5.14 Timer

The timer consists of one advanced 16-bit timer, three general-purpose 16-bit timers, two watchdog timers and one system time base timer.

1.5.14.1 Advanced Control Timer (TIM1)

The advanced control timer (TIM1) is a 16-bit automatic loading counter with a programmable prescaler. In addition to the complete general timer function, it can be regarded as a three-phase PWM generator assigned to six channels, having the complementary PWM output function with dead zone insertion. The timer allows to be updated after a specified number of counter cycles for repeated counting cycle and braking function, etc. Many functions of advanced control timer are the same as those of general timer, and the internal structure is also the same. Therefore, advanced control timer can operate with TIM timer through timer link function to provide synchronization or event linking function.

1.5.14.2 General-purpose Timer (TIM2/3/4)

The system is provided with up to 3 standard timers (TIM2, TIM3 and TIM4) which can be operated synchronously. Each timer has a 16-bit auto-load increment / decrement counter, a programmable 16-bit prescaler and four independent channels, each of which can be used for input capture, output comparison, PWM generation and single pulse mode output.

It can also work with advanced control timer through timer link function to provide synchronization or event linking function. In the debug mode, the counter can be frozen and the PWM output is disabled, thus switching off the switches controlled by these outputs. Any general-purpose timer can be used to generate PWM output. Each timer has its own DMA request mechanism.

These timers can also process signals from incremental encoders and digital outputs from one to three Hall sensors.

1.5.14.3 Independent watchdog (IWDG)

The independent watchdog is a free running 12-bit down counter with an 8-bit prescaler. The clock is provided by an internally independent 40KHz RC oscillator; since this RC oscillator is independent of the master clock, it can operate in stop and standby modes. IWDG completely works independently of the main program, so it can be used to reset the whole system in case of problems, or to provide timeout management for applications as a free timer. The option byte can be configured as a software or hardware boot watchdog. In the debug mode, the counter can be frozen.

1.5.14.4 Window Watchdog (WWDG)

The window watchdog is a 7-bit down counter and can be set to run freely. It can be used to reset the entire system in the event of a problem. It is driven by the master clock and has the function of early warning interrupt. In the debug mode, the counter can be frozen.

1.5.14.5 System Time Base Timer (SysTick)

This is a timer provided by the core controller to generate SYSTICK exception. It can be used in real-time operating system to provide "heartbeat" rhythm for the system. It can also be used as a standard 64-bit increment counter. The 8 frequency divisions of AHB clock are used as the reference clock sources. When the counter is increased to the set comparison value, a maskable system interrupt will be generated.

1.5.15 Standard Communication Interface

1.5.15.1 Universal Synchronous Asynchronous Receiver / Transmitter (USART)

Three groups of USARTs support full duplex asynchronous communication, synchronous one-way communication, half duplex single line communication, Lin (local Internet), and are compatible with smart card

protocol of ISO7816, IrDA SIR ENDEC transmission coding and decoding specifications, and modem (CTS / RTS hardware flow control) operation. The multi-processor communication is also allowed. The fractional baud rate generator system is used. The baud rate of USART1 is up to 4.5Mbits/s, and baud rate of USART2/3 can be up to 2.25Mbits/s. They support DMA operation for continuous communication.

1.5.15.2 Serial Peripheral Interface (SPI)

Two sets of SPIs provide the master or slave operation and are switched dynamically. They support multi-master mode, full duplex or half duplex synchronous transmission, and support basic SD card and MMC mode. The clock frequency is up to 36MHz, clock polarity and phase are programmable, 8-bit or 16-bit data bit width is optional, the hardware CRC generation / verification has reliable communication and DMA operation continuous communication is supported.

1.5.15.3 I2C Bus

Up to two I2Cs can work in multi-host mode or slave mode and complete specific timing, protocol, arbitration, etc. for the all I2C buses. They support standard and fast communication speed, and are compatible with SMBus2.0 etc.

I2Cs provide 7-bit or 10-bit addressing, and support dual-slave addressing in 7-bit slave mode. The built-in hardware CRC generator / calibrator have been provided. DMA can be used to operate and support SMBus bus version 2.0 / PMBus bus.

1.5.15.4 Universal Serial Bus (USB)

The product is embedded with a USB2.0 host controller and device controller (USBHD), which comply with USB2.0 Fullspeed standard. It provides 16 configurable USB device endpoints and a set of host endpoints. It supports control / batch / synchronous / interrupt transmission, double buffer area mechanism, USB bus suspension / operation resumption, and provides standby / wake-up function. The dedicated 48MHz clock of USBHD module is directly generated by internal main PLL frequency division (PLL must be 72MHz or 48MHz).

1.5.16 General-purpose Input/ Output (GPIO)

The system provides 4 groups of GPIO ports with 51 GPIO pins in total. Each pin can be configured as an output (push-pull or open drain), an input (with or without pull-up or pull-down) or a multiplexed peripheral function port by software. Most GPIO pins can be shared with digital or analog multiplexed peripherals. Except for the ports with analog input function, all GPIO pins have high current carrying capacity. It provides a locking mechanism to freeze IO configuration to avoid accidental writing to I / O register.

1.5.17 2-Wire Serial Debugging Interface (SWD)

The embedded SWD interface is a 2-wire serial debugging interface. It includes SWDIO and SWCLK pins in hardware terms, and support online code upgrade and debug.

Chapter 2 Pin Information

2.1 Pins Arrangement

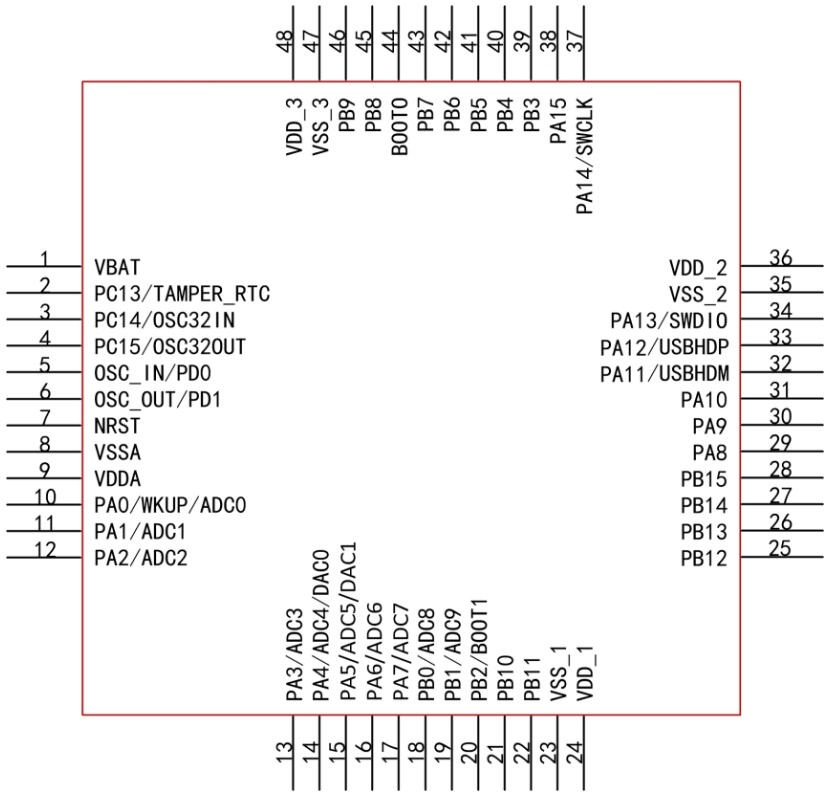

Figure 2-1 CH32V103Cx (LQFP48/QFN48X7) Pin Arrangement

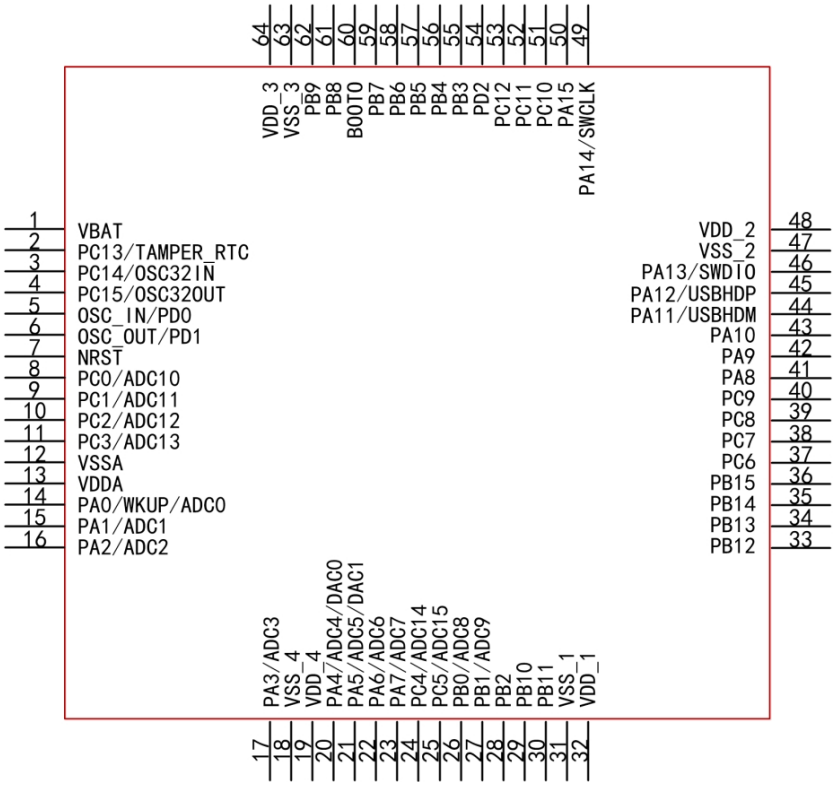

Figure 2-2 CH32V103Rx (LQFP64M) Pin Arrangement

2.2 Description of Pin

Table 2-1 Definition of CH32V103x8x6 Pin

Pin No.			Pin Name	Pin Type	Main function (After reset)	Default multiplex function	Remapping function
LQFP48	QFN48X7	LQFP64M					
1	1	1	V_{BAT}	P	V_{BAT}		
2	2	2	PC13-TAMPER-RTC	I/O	PC13	TAMPER-RTC	
3	3	3	PC14-OSC32_IN	I/O/A	PC14	OSC32_IN	
4	4	4	PC15-OSC32_OUT	I/O/A	PC15	OSC32_OUT	
5	5	5	OSC_IN	I/A	OSC_IN		PD0
6	6	6	OSC_OUT	O/A	OSC_OUT		PD1
7	7	7	NRST	I/O	NRST		
-	-	8	PC0	I/O/A	PC0	ADC_IN10	
-	-	9	PC1	I/O/A	PC1	ADC_IN11	
-	-	10	PC2	I/O/A	PC2	ADC_IN12	
-	-	11	PC3	I/O/A	PC3	ADC_IN13	
8	8	12	V_{SSA}	P	V_{SSA}		
9	9	13	V_{DDA}	P	V_{DDA}		
10	10	14	PA0-WKUP	I/O/A	PA0	WKUP/USART2_CTS /ADC_IN0/TIM2_CH1 /TIM2_ETR	
11	11	15	PA1	I/O/A	PA1	USART2_RTS/ADC_IN1 /TIM2_CH2	
12	12	16	PA2	I/O/A	PA2	USART2_TX/ADC_IN2 /TIM2_CH3	
13	13	17	PA3	I/O/A	PA3	USART2_RX/ADC_IN3 /TIM2_CH4	
-	-	18	V_{SS_4}	P	V_{SS_4}		
-	-	19	V_{DD_4}	P	V_{DD_4}		
14	14	20	PA4	I/O/A	PA4	SPI1_NSS/USART2_CK /ADC_IN4	
15	15	21	PA5	I/O/A	PA5	SPI1_SCK/ADC_IN5	
16	16	22	PA6	I/O/A	PA6	SPI1_MISO/ADC_IN6 /TIM3_CH1	TIM1_BKIN
17	17	23	PA7	I/O/A	PA7	SPI1_MOSI/ADC_IN7 /TIM3_CH2	TIM1_CH1N
-	-	24	PC4	I/O/A	PC4	ADC_IN14	
-	-	25	PC5	I/O/A	PC5	ADC_IN15	

18	18	26	PB0	I/O/A	PB0	ADC_IN8/TIM3_CH3	TIM1_CH2N
19	19	27	PB1	I/O/A	PB1	ADC_IN9/TIM3_CH4	TIM1_CH3N
20	20	28	PB2	I/O	PB2 /BOOT1		
21	21	29	PB10	I/O	PB10	I2C2_SCL/USART3_TX	TIM2_CH3
22	22	30	PB11	I/O	PB11	I2C2_SDA/USART3_RX	TIM2_CH4
23	23	31	V_{SS_1}	P	V_{SS_1}		
24	24	32	V_{DD_1}	P	V_{DD_1}		
25	25	33	PB12	I/O	PB12	SPI2_NSS/I2C2_SMBAI /USART3_CK/TIM1_BKIN	
26	26	34	PB13	I/O	PB13	SPI2_SCK/USART3_CTS /TIM1_CH1N	
27	27	35	PB14	I/O	PB14	SPI2_MISO/USART3_RTS /TIM1_CH2N	
28	28	36	PB15	I/O	PB15	SPI2_MOSI/TIM1_CH3N	
-	-	37	PC6	I/O	PC6		TIM3_CH1
-	-	38	PC7	I/O	PC7		TIM3_CH2
-	-	39	PC8	I/O	PC8		TIM3_CH3
-	-	40	PC9	I/O	PC9		TIM3_CH4
29	29	41	PA8	I/O	PA8	USART1_CK/TIM1_CH1 /MCO	
30	30	42	PA9	I/O	PA9	USART1_TX/TIM1_CH2	
31	31	43	PA10	I/O	PA10	USART1_RX/TIM1_CH3	
32	32	44	PA11	I/O/A	PA11	USART1_CTS/USBHDM /TIM1_CH4	
33	33	45	PA12	I/O/A	PA12	USART1_RTS/USBHDP /TIM1_ETR	
34	34	46	PA13	I/O	SWDIO		PA13
35	35	47	V_{SS_2}	P	V_{SS_2}		
36	36	48	V_{DD_2}	P	V_{DD_2}		
37	37	49	PA14	I/O	SWCLK		PA14
38	38	50	PA15	I/O	PA15		TIM2_CH1 /TIM2_ETR /SPI1_NSS
-	-	51	PC10	I/O	PC10		UASRT3_TX
-	-	52	PC11	I/O	PC11		USART3_RX
-	-	53	PC12	I/O	PC12		USART3_CK
-	-	54	PD2	I/O	PD2	TIM3_ETR	
39	39	55	PB3	I/O	PB3		TRACESWO /TIM2_CH2 /SPI1_SCK
40	40	56	PB4	I/O	PB4		TIM3_CH1 /SPI1_MISO
41	41	57	PB5	I/O	PB5	I2C1_SMBAI	TIM3_CH2

							/SPI1_MOSI
42	42	58	PB6	I/O/A	PB6	I2C1_SCL/TIM4_CH1	USART1_TX
43	43	59	PB7	I/O/A	PB7	I2C1_SDA/TIM4_CH2	USART1_RX
44	44	60	BOOT0	I	BOOT0		
45	45	61	PB8	I/O/A	PB8	TIM4_CH3	I2C1_SCL
46	46	62	PB9	I/O/A	PB9	TIM4_CH4	I2C1_SDA
47	47	63	V_{SS_3}	P	V_{SS_3}		
48	48	64	V_{DD_3}	P	V_{DD_3}		

Table 2-2 Definition of CH32V103x6x6 Pin

Pin No.		Pin Name	Pin Type	Main function (After reset)	Default multiplex function	Remapping function
LQFP48	LQFP64M					
1	1	V_{BAT}	P	V_{BAT}		
2	2	PC13-TAMPER-RTC	I/O	PC13	TAMPER-RTC	
3	3	PC14-OSC32_IN	I/O/A	PC14	OSC32_IN	
4	4	PC15-OSC32_OUT	I/O/A	PC15	OSC32_OUT	
5	5	OSC8M_IN	I/A	OSC8M_IN		PD0
6	6	OSC8M_OUT	O/A	OSC8M_OUT		PD1
7	7	NRST	I/O	NRST		
-	8	PC0	I/O/A	PC0	ADC_IN10	
-	9	PC1	I/O/A	PC1	ADC_IN11	
-	10	PC2	I/O/A	PC2	ADC_IN12	
-	11	PC3	I/O/A	PC3	ADC_IN13	
8	12	V_{SSA}	P	V_{SSA}		
9	13	V_{DDA}	P	V_{DDA}		
10	14	PA0-WKUP	I/O/A	PA0	WKUP/USART2_CTS /ADC_IN0/TIM2_CH1 /TIM2_ETR	
11	15	PA1	I/O/A	PA1	USART2_RTS/ADC_IN1 /TIM2_CH2	
12	16	PA2	I/O/A	PA2	USART2_TX/ADC_IN2 /TIM2_CH3	
13	17	PA3	I/O/A	PA3	USART2_RX/ADC_IN3 /TIM2_CH4	
-	18	V_{SS_4}	P	V_{SS_4}		
-	19	V_{DD_4}	P	V_{DD_4}		
14	20	PA4	I/O/A	PA4	SPI1_NSS/USART2_CK	

					/ADC_IN4	
15	21	PA5	I/O/A	PA5	SPI1_SCK/ADC_IN5	
16	22	PA6	I/O/A	PA6	SPI1_MISO/ADC_IN6 /TIM3_CH1	TIM1_BKIN
17	23	PA7	I/O/A	PA7	SPI1_MOSI/ADC_IN7 /TIM3_CH2	TIM1_CH1N
-	24	PC4	I/O/A	PC4	ADC_IN14	
-	25	PC5	I/O/A	PC5	ADC_IN15	
18	26	PB0	I/O/A	PB0	ADC_IN8/TIM3_CH3	TIM1_CH2N
19	27	PB1	I/O/A	PB1	ADC_IN9/TIM3_CH4	TIM1_CH3N
20	28	PB2	I/O	PB2/BOOT1		
21	29	PB10	I/O	PB10		TIM2_CH3
22	30	PB11	I/O	PB11		TIM2_CH4
23	31	V_{SS_1}	P	V_{SS_1}		
24	32	V_{DD_1}	P	V_{DD_1}		
25	33	PB12	I/O	PB12	TIM1_BKIN	
26	34	PB13	I/O	PB13	TIM1_CH1N	
27	35	PB14	I/O	PB14	TIM1_CH2N	
28	36	PB15	I/O	PB15	TIM1_CH3N	
-	37	PC6	I/O	PC6		TIM3_CH1
-	38	PC7	I/O	PC7		TIM3_CH2
-	39	PC8	I/O	PC8		TIM3_CH3
-	40	PC9	I/O	PC9		TIM3_CH4
29	41	PA8	I/O	PA8	USART1_CK/TIM1_CH1 /MCO	
30	42	PA9	I/O	PA9	USART1_TX/TIM1_CH2	
31	43	PA10	I/O	PA10	USART1_RX/TIM1_CH3	
32	44	PA11	I/O/A	PA11	USART1_CTS/USBHDM /TIM1_CH4	
33	45	PA12	I/O/A	PA12	USART1_RTS/USBHDP/ TIM1_ETR	
34	46	PA13	I/O	SWDIO		PA13
35	47	V_{SS_2}	P	V_{SS_2}		
36	48	V_{DD_2}	P	V_{DD_2}		
37	49	PA14	I/O	SWCLK		PA14
38	50	PA15	I/O	PA15		TIM2_CH1 /TIM2_ETR /SPI1_NSS
-	51	PC10	I/O	PC10		
-	52	PC11	I/O	PC11		
-	53	PC12	I/O	PC12		
-	54	PD2	I/O	PD2	TIM3_ETR	
39	55	PB3	I/O	PB3		TRACESWO

						/TIM2_CH2 /SPI1_SCK
40	56	PB4	I/O	PB4		TIM3_CH1 /SPI1_MISO
41	57	PB5	I/O	PB5	I2C1_SMBAI	TIM3_CH2 /SPI1_MOSI
42	58	PB6	I/O/A	PB6	I2C1_SCL	USART1_TX
43	59	PB7	I/O/A	PB7	I2C1_SDA	USART1_RX
44	60	BOOT0	I	BOOT0		
45	61	PB8	I/O/A	PB8		I2C1_SCL
46	62	PB9	I/O/A	PB9		I2C1_SDA
47	63	V_{SS_3}	P	V_{SS_3}		
48	64	V_{DD_3}	P	V_{DD_3}		

Notes: Pin type:

I=TTL/CMOS level Schmitt input;

O=CMOS level three-state output;

A=Analog signal input or output;

P= Power supply;

Chapter 3 Electrical Characteristics

3.1 Test Conditions

Unless otherwise specified and indicated, all voltages are referenced to V_{SS}.

All minimum and maximum values will be guaranteed in the worst conditions of ambient temperature, supply voltage and clock frequency. Typical values are based on the normal temperature and V_{DD} = 3.3V, and can be used for design guidance.

Data obtained through comprehensive evaluation, design simulation or process characteristics will not be tested on the production line. Based on the statistical evaluation, the minimum and maximum sample values are obtained through statistics after the sample test.

Normal temperature: 25℃
Power supply scheme:

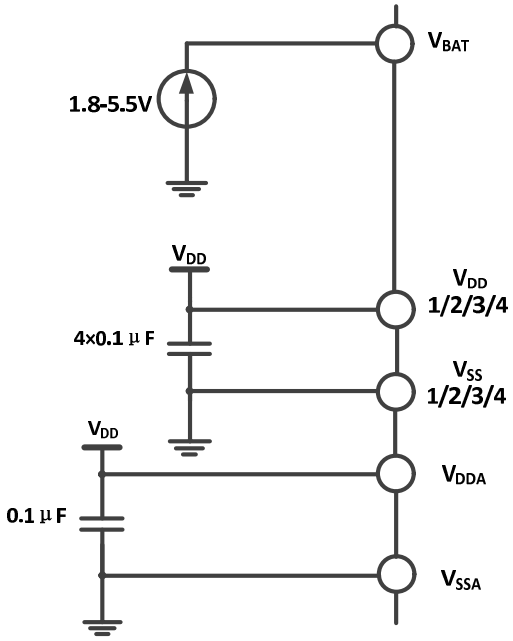

Figure 3-1 Typical Circuit for Conventional Power Supply

3.2 Absolute Maximum Value

Critical value or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged.

Table 3-1 Absolute Maximum Value Parameters

Name	Description	Min.	Max.	Unit
T_A[1]	Ambient temperature during operation	-40	85	℃
T_S	Ambient temperature during storage	-40	105	℃
V_{DD}-V_{SS}[1]	External main supply voltage (including V_{DDA} and V_{DD})	-0.3	5.5	V
V_{IN}[1]	Input voltage on the pin	V_{SS}-0.3	5.5	V

$\|\triangle V_{DDx}\|^1$	Voltage difference between different power supply pins		50	mV
$\|V_{SSx}-V_{SS}\|^1$	Voltage difference between different grounding pins		50	mV
$V_{ESD(HBM)}^1$	ESD voltage (human model, non-contact type)	4000		V
I_{VDD}^2	Total current through V_{DD}/V_{DDA} power line (supply current)		50	mA
I_{Vss}^2	Total current through V_{SS} ground (outflow current)		50	
I_{IO}^1	Draw current on any I/O and control pin		-25	
	Output current on any I/O and control pin		25	

Notes: 1. Design parameters.

2. The maximum current value can be reached in normal operation.

3.3 Electrical parameters

3.3.1 Operating conditions

Table 3-2 General Operating conditions

Name	Parameter	Condition	Min.	Max.	Unit
F_{SYSCLK}	Internal system clock frequency			80	MHz
F_{HCLK}	Internal AHB domain bus clock frequency			80	MHz
F_{PCLK1}	Internal APB1 domain bus clock frequency			80	MHz
F_{PCLK2}	Internal APB2 domain bus clock frequency			80	MHz
V_{DD}	Standard operating voltage		2.7	5.5	V
V_{DDA}	Operating voltage of analog part (ADC is not used)	It must be the same as V_{DD}.	2.7	5.5	V
	Operating voltage of analog part (ADC is used)		3.0		
V_{BAT}^2	Operating voltage of backup unit	It cannot be greater than V_{DD}	1.8	5.5	V
T_A^1	Ambient temperature		-40	85	℃

Notes: 1. Design parameters.

2. The connecting line from the battery to V_{BAT} shall be as short as possible.

Table 3-3 Power-up and Power-down Conditions

Name	Parameter	Condition	Min.	Max.	Unit
t_{VDD}	VDD rise time rate		0	∞	us/V
	VDD fall time rate		50	∞	us/V

Note: The connecting line from the battery to N_{BAT} shall be as short as possible.

3.3.2 Embedded Reset and Power Control Module Features

Table 3-4 Reset and Voltage Monitor

Name	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{PVD}[2]	Electric level selection of programmable voltage detector	PLS[2:0] = 000 (rising edge)		2.65		V
		PLS[2:0] = 000 (falling edge)		2.5		V
		PLS[2:0] = 001 (rising edge)		2.87		V
		PLS[2:0] = 001 (falling edge)		2.7		V
		PLS[2:0] = 010 (rising edge)		3.07		V
		PLS[2:0] = 010 (falling edge)		2.89		V
		PLS[2:0] = 011 (rising edge)		3.27		V
		PLS[2:0] = 011 (falling edge)		3.08		V
		PLS[2:0] = 100 (rising edge)		3.46		V
		PLS[2:0] = 100 (falling edge)		3.27		V
		PLS[2:0] = 101 (rising edge)		3.76		V
		PLS[2:0] = 101 (falling edge)		3.55		V
		PLS[2:0] = 110 (rising edge)		4.07		V
		PLS[2:0] = 110 (falling edge)		3.84		V
		PLS[2:0] = 111 (rising edge)		4.43		V
		PLS[2:0] =111 (falling edge)		4.18		V
$V_{PVDhyst}$[1]	PVD hysteresis			0.2		V
$V_{POR/PDR}$[1]	Power-up/power-down reset threshold	Rising edge		2.5		V
		Falling edge		2.42		V
$V_{PDRhyst}$[1]	PDR hysteresis		40		110	mV
$t_{RSTTEMPO}$[1]	Reset duration		16		44	mS

Notes: 1. Design parameters.

2. Room-temperature test value.

3.3.3 Built-in Reference Voltage

Table 3-5 Built-in Reference Voltage

Name	Parameter	Condition	Min.	Max.	Unit
V_{REFINT}	Built-in reference voltage	T_A = -40℃～85℃	1.12	1.28	V
$T_{S\_vrefint}$	Sample time of ADC when reading out internal reference voltage		0.107	17.1	us

3.3.4 Supply Current Characteristics

Current consumption is a comprehensive index of multiple parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin flip rate, and program location in memory and executed code, etc.

The current consumption measurement method is as shown in the figure below:

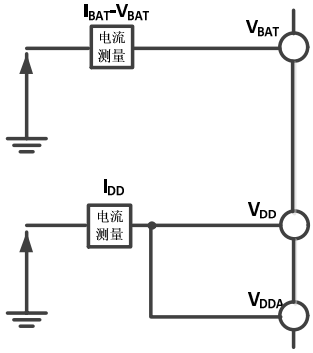

Figure 3-2 Current Consumption Measurement

The microcontroller is under the following conditions:
Under normal temperature conditions, V_{DD} = 3.3V, and all IO ports are configured with pull-up inputs, all peripheral clocks (excluding GPIO peripherals) are enabled or disabled, and peripheral functions are not initialized.

Table 3-6 Typical Current Consumption in run mode, data processing codes run in internal flash memory

Name	Parameter	Condition		Typ.		Unit
				Enable all peripherals	Disable all peripherals	
I_{DD}	Supply current in run mode	External clock	F_{SYSCLK} = 72MHz	13.56	8.88	mA
			F_{SYSCLK} = 48MHz	9.76	6.64	
			F_{SYSCLK} = 36MHz	8.51	5.85	
			F_{SYSCLK} = 24MHz	6.38	4.62	
			F_{SYSCLK} = 16MHz	5.11	3.88	
			F_{SYSCLK} = 8MHz	3.15	2.61	
			F_{SYSCLK} = 4MHz	2.50	2.26	
			F_{SYSCLK} = 500KHz	1.99	1.96	
		Run in high-speed internal RC oscillator (HSI), and use AHB prescaler to reduce frequency	F_{SYSCLK} = 64MHz	12.63	7.63	
			F_{SYSCLK} = 48MHz	9.92	6.17	
			F_{SYSCLK} = 36MHz	7.90	5.08	
			F_{SYSCLK} = 24MHz	5.75	3.98	
			F_{SYSCLK} = 16MHz	4.57	3.31	
			F_{SYSCLK} = 8MHz	2.82	2.23	
			F_{SYSCLK} = 4MHz	2.19	1.88	
			F_{SYSCLK} = 500KHz	1.61	1.58	

Note: The parameters above are actually measured.

Table 3-7 Typical Current Consumption in Sleep mode, data processing codes run in internal flash memory or SRAM.

Name	Parameter	Condition		Typ.		Unit
				Enable all peripherals	Disable all peripherals	
I_{DD}	Supply current in sleep mode (At this time, peripheral power supply and clock are maintained)	External clock	F_{SYSCLK} = 72MHz	10.98	5.33	mA
			F_{SYSCLK} = 48MHz	8.05	4.27	
			F_{SYSCLK} = 36MHz	6.87	4.06	
			F_{SYSCLK} = 24MHz	5.30	3.42	
			F_{SYSCLK} = 16MHz	4.34	3.08	
			F_{SYSCLK} = 8MHz	2.83	2.21	
			F_{SYSCLK} = 4MHz	2.37	2.06	
			F_{SYSCLK} = 500KHz	1.97	1.93	
		Run in high-speed internal RC oscillator (HSI), and use AHB prescaler to reduce frequency	F_{SYSCLK} = 64MHz	9.71	4.69	
			F_{SYSCLK} = 48MHz	7.73	3.96	
			F_{SYSCLK} = 36MHz	6.24	3.41	
			F_{SYSCLK} = 24MHz	4.76	2.87	
			F_{SYSCLK} = 16MHz	3.83	2.57	
			F_{SYSCLK} = 8MHz	2.47	1.84	
			F_{SYSCLK} = 4MHz	2.00	1.68	
			F_{SYSCLK} = 500KHz	1.59	1.55	

Note: The parameters above are actually measured.

Table 3-8 Typical Current Consumption in Stop and Standby Modes

Name	Parameter	Condition	Typ.	Unit
I_{DD}	Supply current in stop mode	The voltage regulator is in the running mode, and the low-speed and high-speed internal RC oscillators and external oscillators are both at the off state (no independent watchdog)	455	uA
		The voltage regulator is in low power consumption mode, and the low-speed and high-speed internal RC oscillators and external oscillators are off (no independent watchdog)	1.6	
	Supply current in standby mode	Low-speed internal RC oscillator and independent watchdog are on	2.8	
		The low-speed internal RC oscillator is on, and the independent watchdog is off	2.7	

		The low-speed internal RC oscillator and the independent watchdog are off.	1.6	
I_{DD_VBAT}	The supply current in the backup area (V_{DD} and V_{DDA} are removed, and only V_{BAT} is used to supply power)	Low-speed external oscillator and RTC are on	2.4	

Note: The parameters above are actually measured.

3.3.5 External Clock Source Characteristics

Table 3-9 From External High-speed Clock

Name	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSE_ext}	External clock frequency			8	25	MHz
V_{HSEH}[1]	OSC_IN input pin high-level voltage		$0.8V_{DD}$		V_{DD}	V
V_{HSEL}[1]	OSC_IN input pin low-level voltage		0		$0.2V_{DD}$	V
$C_{in(HSE)}$	OSC_IN input capacitance			5		pF
$DuCy_{(HSE)}$	Duty cycle			50		%

Note: 1. Failure to meet this condition may cause level recognition errors.

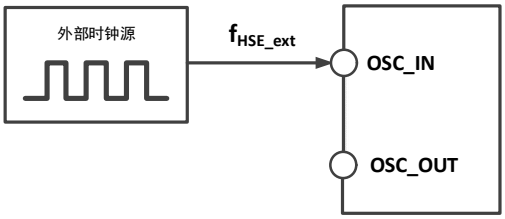

Figure 3-3 Circuit for Providing High-Frequency Clock Source Externally

Table 3-10 From External Low-speed Clock

Name	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LSE_ext}	User's external clock frequency			32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin high-level voltage		$0.8V_{DD}$		V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		0		$0.2V_{DD}$	V
$C_{in(LSE)}$	OSC32_IN input capacitance			5		pF
$DuCy_{(LSE)}$	Duty cycle			50		%

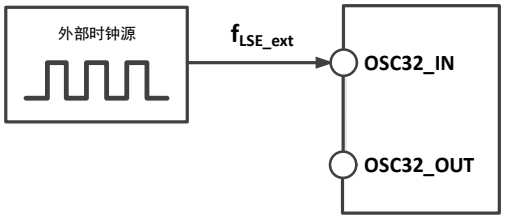

Figure 3-4 Circuit for Providing Low-Frequency Clock Source Externally

Table 3-11 High-Speed External Clock Using a Crystal/Ceramic Resonator

Name	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{OSC_IN}	Resonator frequency		4	8	16	MHz
I_2[1]	HSE driving current	V_{DD} = 3.3V，20p load		0.2		mA
g_m[1]	Transconductance of the oscillator	Start		4.6		mA/V
$t_{SU(HSE)}$	Startup time	V DD is stable		1		ms

Notes: 1. Design parameters.

Circuit reference design and requirements:

The selected load capacitance of the crystal is generally 20pF (C_{L1}=C_{L2}, recommended 5～25pF). Please refer to the data manual of the crystal manufacturer specifically.

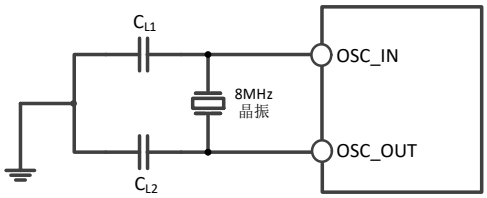

Figure 3-5 Typical Circuit with an External 8M Crystal

Table 3-12 Low-Speed External Clock Generated by a Crystal/Ceramic Resonator ($f_{(LSE)}$=32.768KHz)

Name	Parameter	Condition	Min.	Typ.	Max.	Unit
i_2[1]	LSE driving current	V_{DD} = 3.3V		0.5		uA
g_m[1]	Transconductance of the oscillator	Start		13.5		uA/V
$t_{SU(LSE)}$	Startup time	V DD is stable		200		mS

Notes: 1. Design parameters.

Circuit reference design and requirements:

The selected load capacitance of the crystal generally shall not exceed 15pF (C_{L1} =C_{L2} , recommended 5～15pF). Please refer to the data manual of the crystal manufacturer specifically.

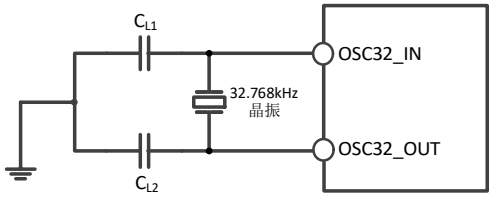

Figure 3-6 Typical Circuit of External 32.768K Crystal

Note: The load capacitance C_L is calculated by the following formula: C_L = C_{L1} x C_{L2} / (C_{L1} + C_{L2}) + C_{stray}, whereof C_{stray} is the capacitance of the pin and the related capacitance of PCB board or PCB. Its typical value is between 2pF and 7pF.

3.3.6 Internal Clock Source Characteristics

Table 3-13 Internal High-Speed (HSI) RC Oscillator Characteristics

Name	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSI}	Frequency			8		MHz
$DuCy_{HSI}$	Duty cycle		45	50	55	%
ACC_{HSI}	Accuracy of HSI oscillator	T_A = 0℃～70℃	-1.5		1.5	%
		T_A = -40℃～85℃	-2		2	%
$t_{SU(HSI)}$	Startup time of HSI oscillator				2.6	us
$I_{DD(HSI)}$	Power consumption of HSI oscillator			200		uA

Table 3-14 Internal Low-Speed (LSI) RC Oscillator Characteristics

Name	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LSI}	Frequency		25	36	60	KHz
$DuCy_{LSI}$	Duty cycle		45	50	55	%
$t_{SU(LSI)}$	Startup time of LSI oscillator				82	us
$I_{DD(LSI)}$[1]	Power consumption of LSI oscillator			0.6		uA

Notes: 1. Design parameters.

3.3.7 PLL Characteristics

Table 3-15 PLL Characteristics

Name	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{PLL_IN}	PLL input clock		4	8	16	MHz
	PLL input clock duty cycle [1]		40		60	%
F_{PLL_OUT}	PLL multiplier output clock				80	MHz
t_{LOCK}[1]	PLL lock time				1000	$1/F_{PLL\_IN}$

Notes: 1. Design parameters.

3.3.8 Time to Wake up from Low Power Mode

Table 3-16 Time to Wake up from Low Power Mode

Name	Parameter	Condition	Typ.	Unit
$t_{wusleep}$	Wake up from sleep mode	Wake up using the HSI RC clock	5.8	us
t_{wustop}	Wake up from stop mode (voltage regulator is in run mode)	HSI RC clock wake-up	253	us
	Wake up from the stop mode (voltage regulator is in the low power mode)	Time to wake voltage regulator up from low power mode + HSI RC clock wake-up + flash start	253	us
$t_{WUSTDBY}$	Wake up from standby mode	Time to wake voltage regulator up from low power consumption mode + HSI RC clock wake-up + flash start	340	us

3.3.9 Memory Characteristics

Table 3-17 Flash Memory Characteristics

Name	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{ERASE_128}	Page (128 bytes) programming time	T_A = -40℃～85℃	2.5	2.75	3	ms
t_{ERASE}	Page (128 bytes) erasing time	T_A = -40℃～85℃	2.5	2.75	3	ms
t_{prog}	16-bit programming time	T_A = -40℃～85℃	2.5	2.75	3	ms
t_{ERASE}	Page (1K bytes) erasure time	T_A = -40℃～85℃	20	22	24	ms
t_{ME}	Whole erasure time	T_A = -40℃～85℃	2.5	2.75	3	ms
V_{prog}	Programming voltage		2.7		5.5	V

Table 3-18 Flash Memory Life and Data Retention Period

Name	Parameter	Condition	Min.	Typ.	Max.	Unit
N_{END}	Number of erasure/programming	T_A = 25℃	10K	80K[1]		Time
t_{RET}	Data retention period		10			Year

Note: The number of erasure/programming operations is actually measured, not guaranteed.

3.3.10 I/O Port Characteristics

Table 3-19 General-purpose I/O Static Characteristics

Name	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage	TTL port	-0.3		0.8	V
V_{IH}	Standard I/O pin, input high level voltage	TTL port 2.7V<V_{DD}<4.2V	2		V_{DD}+0.3	V
		TTL port 4.2V≤V_{DD}<5.5V	0.55V_{DD}		V_{DD}+0.3	V
V_{IL}	Input low level voltage	CMOS port	-0.3		0.8	V
V_{IH}	Input high level voltage		0.65V_{DD}		V_{DD}+0.3	V
V_{hys}	Schmitt trigger voltage hysteresis for standard I/O pin			330		mV
I_{lkg}	Input leakage current				±1	uA
R_{PU}	Weak pull-up equivalent resistance		30	42	55	KΩ
R_{PD}	Weak pull-down equivalent resistance		30	42	55	KΩ
C_{IO}	I/O pin capacitance			5		pF

Note: The parameters provided above are designed.

Output drive current characteristics

GPIO (General-purpose input/output) can absorb or output up to ±8mA current, and absorb or output ±20mA current (not strictly reaching V_{OL}/V_{OH}). In the user applications, the total current driven by all IO pins cannot exceed the absolute maximum ratings provided in section 3.2:

Table 3-20 Output Voltage Characteristics

Name	Parameter	Condition	Min.	Max.	Unit
V_{OL}	Output low level, single-pin draw current	TTL port, I_{IO} = +8mA 2.7V< V_{DD} <5.5V		0.4	V
V_{OH}	Output high level, single pin output current		V_{DD}-0.4		V
V_{OL}	Output low level, single-pin draw current	CMOS port, I_{IO} = +8mA 2.7V< V_{DD} <5.5V		0.4	V
V_{OH}	Output high level, single pin output current		2.3		V
V_{OL}	Output low level, single-pin draw current	I_{IO} = +20mA 2.7V< V_{DD} <5.5V		1.3	V
V_{OH}	Output high level, single pin output current		V_{DD}-1.3		V

Note: In the above conditions, if multiple IO pins are driven at the same time, the total current cannot exceed the absolute maximum ratings given in Table 3.2. In addition, when multiple IO pins are driven at the same time, the current on the power/ground wire point is very large, which will result in the voltage drop to make the internal IO voltage not reach the power supply voltage in the table, causing the drive current to be less than the nominal value.

Table 3-21 Input and Output AC Characteristics

MODEx[1:0] Cinfiguration	Name	Parameter	Condition	Min.	Max.	Unit
10 (2MHz)	$F_{max(IO)out}$	Maximum frequency	CL=50pF,VDD=2.7-5.5V		2	MHz
	$t_{f(IO)out}$	Fall time from output high level to low level	CL=50pF,VDD=2.7-5.5V		125	ns
	$t_{r(IO)out}$	Rise time from output low level to high level			125	ns
01 (10MHz)	$F_{max(IO)out}$	Maximum frequency	CL=50pF,VDD=2.7-5.5V		10	MHz
	$t_{f(IO)out}$	Fall time from output high level to low level	CL=50pF,VDD=2.7-5.5V		25	ns
	$t_{r(IO)out}$	Rise time from output low level to high level			25	ns
11 (50MHz)	$F_{max(IO)out}$	Maximum frequency	CL=30pF,VDD=2.7-5.5V		50	MHz
			CL=50pF,VDD=2.7-5.5V		30	MHz
	$t_{f(IO)out}$	Fall time from output high level to low level	CL=30pF,VDD=2.7-5.5V		20	ns
			CL=50pF,VDD=2.7-5.5V		5	ns
	$t_{r(IO)out}$	Rise time from output low level to high level	CL=30pF,VDD=2.7-5.5V		8	ns
			CL=50pF,VDD=2.7-5.5V		12	ns
	t_{EXTIpw}	Pulse width that EXTI controller detects external signal		10		ns

Note: The parameters provided above are designed.

3.3.11 NRST Pin Characteristics

Table 3-22 External Reset Pin Characteristics

Name	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$[1]	NRST input low voltage		-0.3		0.8	V
$V_{IH(NRST)}$[1]	NRST input high voltage		$0.65V_{DD}$		V_{DD}+0.5	V
$V_{hys(NRST)}$	Voltage hysteresis of NRST Schmitt trigger			330		mV
R_{PU}[2]	Weak pull-up equivalent resistance		30	42	55	KΩ
$T_{F(NRST)}$[1]	NRST input filter pulse				4	ns
$T_{NF(NRST)}$[1]	NRST input unfiltered pulse		20			ns

Notes: 1. Designed parameters.

2. The pull-up resistor is a real resistor connected in series with a switchable PMOS. The resistance of this PMOS/NMOS switch is very small (occupies approximately 10%).

Circuit reference design and requirements:

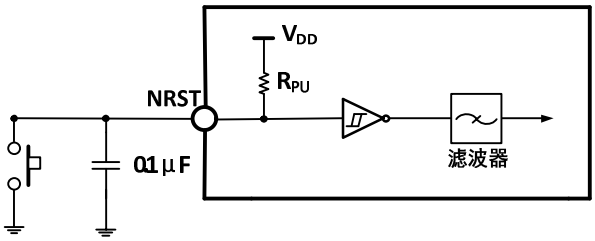

Figure 3-7 Typical Circuit of External Reset Pin

3.3.11 TIM Timer Characteristics

Table 3-23 TIMx Characteristics

Name	Parameter	Condition	Min.	Max.	Unit
$t_{res(TIM)}$	Timer reference clock		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz	13.9		ns
F_{EXT}	External clock frequency of CH1 to CH4 timers		0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$ = 72MHz	0	36	MHz
R_{esTIM}	Timer resolution			16	Bit
$t_{COUNTER}$	The 16-bit counter clock cycle when the internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz	0.0139	910	us
t_{MAX_COUNT}	Maximum possible count			65535	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz		59.6	s

Note: The parameters provided above are designed.

3.3.12 I2C Interface Characteristics

Table 3-24 I2C Interface Characteristics

Name	Parameter	Standard I2C		Fast I2C		Unit
		Min.	Max.	Min.	Max.	
$t_{w(SCLL)}$	SCL clock low-level time	4.7		1.2		us
$t_{w(SCLH)}$	SCL clock high-level time	4.0		0.6		us
$t_{SU(SDA)}$	SDA data setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0		0	900	ns
$t_{r(SDA)}/t_{r(SCL)}$	SDA and SCL rise time		1000	20		ns
$t_{F(SDA)}/t_{F(SCL)}$	SDA and SCL fall time		300			ns
$t_{h(STA)}$	Start condition hold time	4.0		0.6		us
$t_{SU(STA)}$	Repeated start condition setup time	4.7		0.6		us
$t_{SU(STO)}$	Setup time of stop condition	4.0		0.6		us
$t_{w(STO:STA)}$	Time from stop condition to start condition (idle bus)	4.7		1.2		us
C_b	Capacitive load of each bus		400		400	pF

Note: The parameters provided above are designed.

3.3.12 SPI interface Characteristics

Table 3-25 SPI interface Characteristics

Name	Parameter	Condition	Min.	Max.	Unit
f_{SCK}	SPI clock frequency	Master mode		36	MHz
		Slave mode		36	MHz
$t_{r(SCK)}/t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C=30pF		20	ns
$t_{SU(NSS)}$	NSS setup time	Slave mode	$2t_{PCLK}$		ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2t_{PCLK}$		ns
$t_{w(SCKH)}/t_{w(SCKL)}$	SCK high-level and low-level time	Master mode, f_{PCLK} = 36MHz, prescaler factor = 4	40	60	ns
$t_{SU(MI)}$	Data input setup time	Master mode	5		ns
		Slave mode	5		ns
$t_{h(MI)}$	Data input hold time	Master mode	5		ns
		Slave mode	4		ns
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK} = 20MHz	0	$1t_{PCLK}$	ns
$t_{dis(SO)}$	Data output prohibition time	Slave mode	0	10	ns
$t_{V(SO)}$	Effective time of data output	Slave mode (after enabling edge)		25	ns
$t_{V(MO)}$	Effective time of data output	Master mode (after enabling edge)		5	ns
$t_{h(SO)}$	Data output hold time	Slave mode (after enabling edge)	15		ns
$t_{h(MO)}$		Master mode (after enabling edge)	0		ns

3.3.13 USB Interface Characteristics

Table 3-26 USB Module Characteristics

Name	Parameter	Condition	Min.	Max.	Unit.
V_{DD}	USB operating voltage	Disable USB5VSEL control bit	3.0	3.6	V
		Enable USB5VSEL control bit	4.0	5.5	
V_{SE}[1]	Single-ended receiver threshold	V_{DD} = 3.3V	1.2	1.9	V
		V_{DD} = 5V	1.2	2	
V_{OL}	Static output low level			0.3	V
V_{OH}	Static output high level		2.8	3.6	V

Notes: 1. Designed parameters.

3.3.14 12-bit ADC Characteristics

Table 3-27 ADC Characteristics

Name	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage		3.0		5.5	V
f_{ADC}	ADC clock frequency				14	MHz
f_S	Sample rate				1	MHz
f_{TRIG}	External trigger frequency	f_{ADC} = 14MHz			875	KHz
					16	$1/f_{ADC}$
V_{AIN}	Conversion voltage range		0		V_{DDA}	V
R_{AIN}	External input impedance				58	KΩ
R_{ADC}	Sample switch resistance			0.6	0.75	KΩ
C_{ADC}	Internal sample and hold capacitance			30		pF
t_{Iat}	Injection trigger conversion delay	f_{ADC} = 14MHz			0.143	us
					2	$1/f_{ADC}$
t_{Iatr}	Conversional trigger conversion delay	f_{ADC} = 14MHz			0.143	us
					2	$1/f_{ADC}$
t_s	Sample time	f_{ADC} = 14MHz	0.107		17.1	us
			1.5		239.5	$1/f_{ADC}$
t_{STAB}	Power-on time				1	us
t_{CONV}	Total conversion time (including sample time)	f_{ADC} = 14MHz	1		18	us
			14		252	$1/f_{ADC}$

Note: The parameters provided above are designed.

Formula: Maximum R_{AIN}

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln 2^{N+2}} - R_{ADC}$$

The above formula is used to determine the maximum external impedance so that the error can be less than 1/4

LSB. Whereof, N=12 (represents 12-bit resolution).

Table 3-28 Maximum R_{AIN} when f_{ADC} = 14MHz

T_S (cycle)	t_S(us)	Maximum R_{AIN}(KΩ)
1.5	0.11	0 (not recommended)
7.5	0.54	1.1
13.5	0.96	2.6
28.5	2.04	6.2
41.5	2.96	9.4
55.5	3.96	12.9
71.5	5.11	16.8
239.5	17.1	58

Note: The parameters provided above are designed.

C_p represents the parasitic capacitance (about 5pF) between the PCB and the bonding pad, which may be related to the quality of the bonding pad and PCB layout. A larger C_p value will reduce the conversion accuracy, and the solution is to reduce the f_{ADC} value.

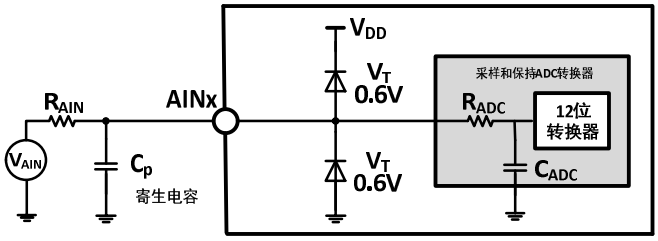

Figure 3-8 Typical Connection Diagram of ADC

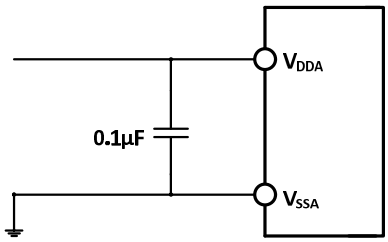

Figure 3-9 Analog Power Supply and Decoupling Circuit Reference

3.3.15 Temperature Sensor Characteristics

Table 3-29 Temperature Sensor Characteristics

Name	Parameter	Condition	Min.	Typ.	Max.	Unit
Avg_Slope	Average slope		3.3	4.3	5.3	mV/℃
V_{25}	Voltage at 25℃		1.11	1.34	1.57	V
T_{S_temp}	ADC sampling time when the temperature is read	f_{ADC} = 14MHz			17.1	us

Note: The parameters provided above are designed.

3.3.16 TKey Module Characteristics

Table 3-29 TKey Module Characteristics

Name	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{TKey}	Working current of module	V_{DD}=3.3V	211	270	421	uA

Chapter 4 Package Information

Chip package

Package	Width of plastic	Pitch of Pin		Instruction Of Package	Ordering Information
LQFP48	7*7mm	0.5mm	19.7mil	Standard LQFP48-pin patch	CH32V103C6T6
LQFP48	7*7mm	0.5mm	19.7mil	Standard LQFP48-pin patch	CH32V103C8T6
QFN48X7	7*7mm	0.5mm	19.7mil	Square leadless 48-pin patch	CH32V103C8U6
LQFP64M	10*10mm	0.5mm	19.7mil	LQFP64M (10*10) patch	CH32V103R8T6

Note: All dimensions are in millimeters, and the pin center spacing is always the nominal value. There is no error, and the other dimension error shall not be more than ±0.4mm or 15%.

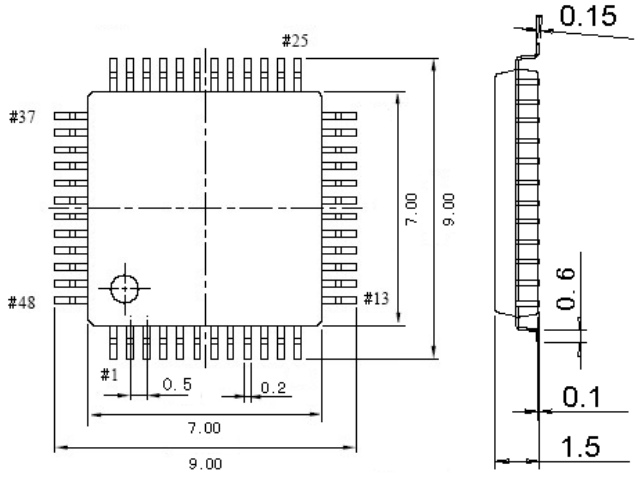

Figure 4-1 LQFP48 Package

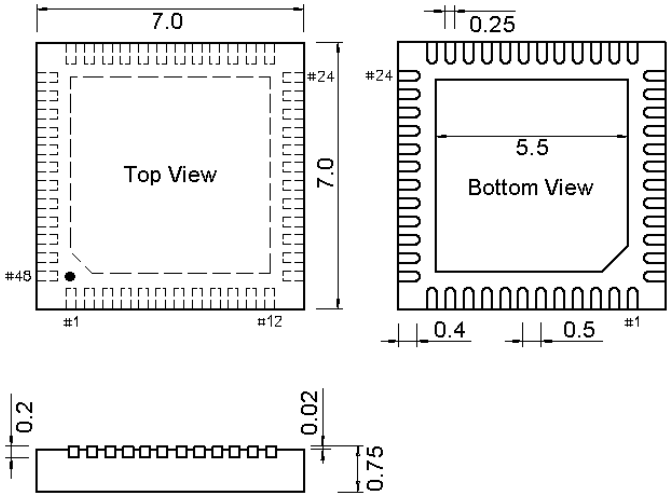

Figure 4-2 QFN48X7 (QFN48-7*7) Package

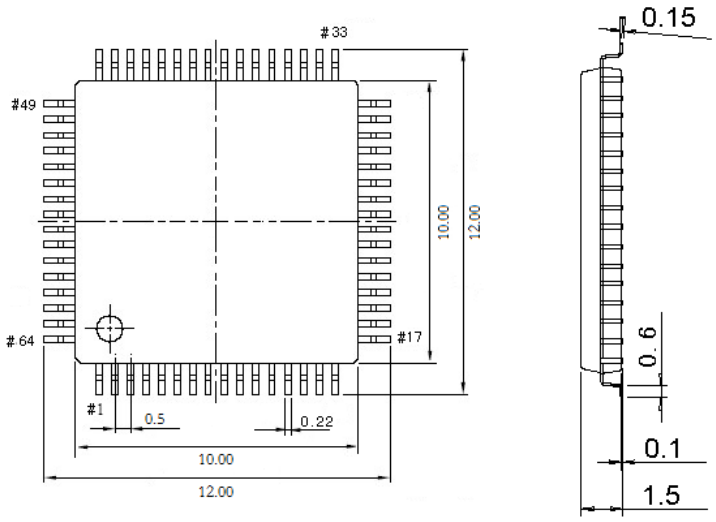

Figure 4-3 LQFP64M (LQFP64-10*10) Package