

**AUTOMOTIVE MOSFET**

**IRFZ44Z**  
**IRFZ44ZS**  
**IRFZ44ZL**

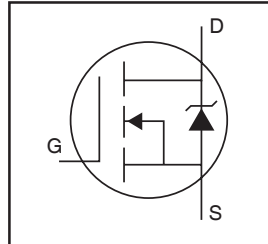
HEXFET® Power MOSFET

**Features**

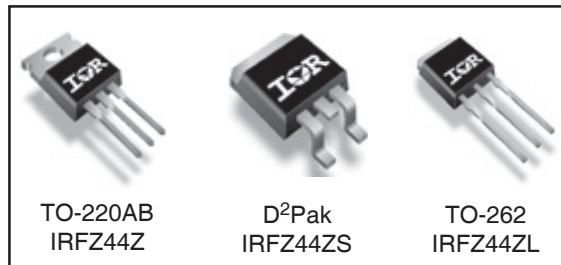
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax

**Description**

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



$V_{DSS} = 55V$
$R_{DS(on)} = 13.9m\Omega$
$I_D = 51A$



**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	51	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (See Fig. 9)	36	
$I_{DM}$	Pulsed Drain Current ①	200	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	80	W
	Linear Derating Factor	0.53	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy (Thermally Limited) ②	86	mJ
$E_{AS} (tested)$	Single Pulse Avalanche Energy Tested Value ②	105	
$I_{AR}$	Avalanche Current ①	See Fig. 12a, 12b, 15, 16	A
$E_{AR}$	Repetitive Avalanche Energy ③		mJ
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

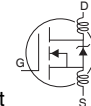
**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.87	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ④	—	40	

HEXFET® is a registered trademark of International Rectifier.

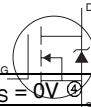
## Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	55	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.054	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	11.1	13.9	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 31A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	22	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 31A
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 55V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 55V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	200	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V <sub>GS</sub> = -20V
Q <sub>g</sub>	Total Gate Charge	—	29	43	nC	I <sub>D</sub> = 31A
Q <sub>gs</sub>	Gate-to-Source Charge	—	7.2	11		V <sub>DS</sub> = 44V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	12	18		V <sub>GS</sub> = 10V ④
t <sub>d(on)</sub>	Turn-On Delay Time	—	14	—	ns	V <sub>DD</sub> = 28V
t <sub>r</sub>	Rise Time	—	68	—		I <sub>D</sub> = 31A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	33	—		R <sub>G</sub> = 15Ω
t <sub>f</sub>	Fall Time	—	41	—		V <sub>GS</sub> = 10V ④
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	1420	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	240	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	130	—		f = 1.0MHz, See Fig. 5
C <sub>oss</sub>	Output Capacitance	—	830	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 1.0V, f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	190	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 44V, f = 1.0MHz
C <sub>oss eff.</sub>	Effective Output Capacitance	—	300	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 44V



## Diode Characteristics

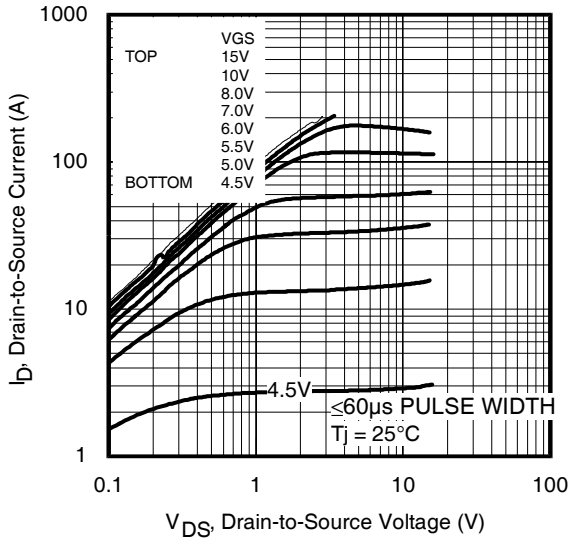
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	51	A	MOSFET symbol showing the integral reverse
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	200		p-n junction diode.
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.2	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 31A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	23	35	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 31A, V <sub>DD</sub> = 28V
Q <sub>rr</sub>	Reverse Recovery Charge	—	17	26	nC	di/dt = 100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				



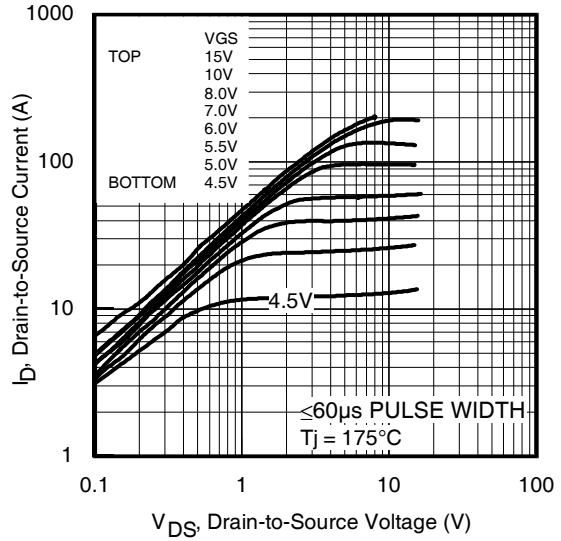
### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.18mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 31A, V<sub>GS</sub> = 10V. Part not recommended for use above this value.
- ③ I<sub>SD</sub> ≤ 31A, di/dt ≤ 840A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C.
- ④ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.

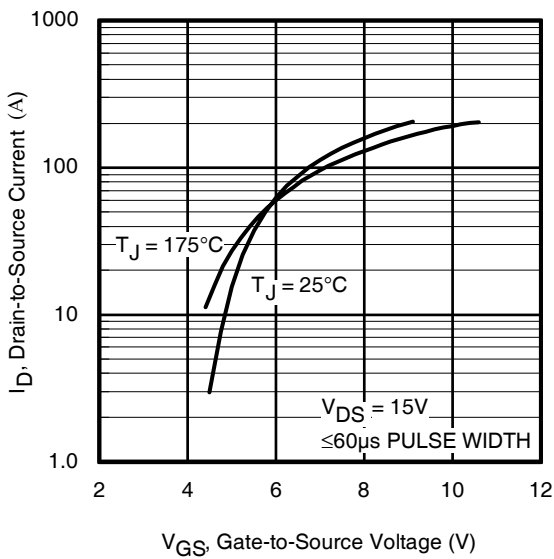
- ⑤ C<sub>oss eff.</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑥ Limited by T<sub>Jmax</sub>, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑦ This value determined from sample failure population. 100% tested to this value in production.
- ⑧ This is applied to D<sup>2</sup>Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ R<sub>θ</sub> is rated at T<sub>J</sub> of approximately 90°C.



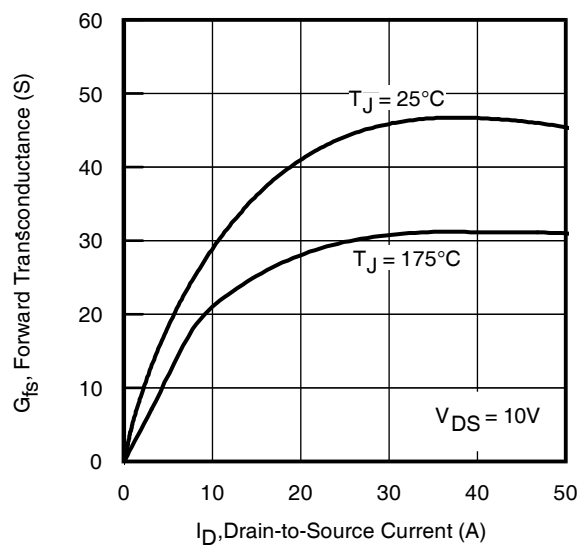
**Fig 1.** Typical Output Characteristics



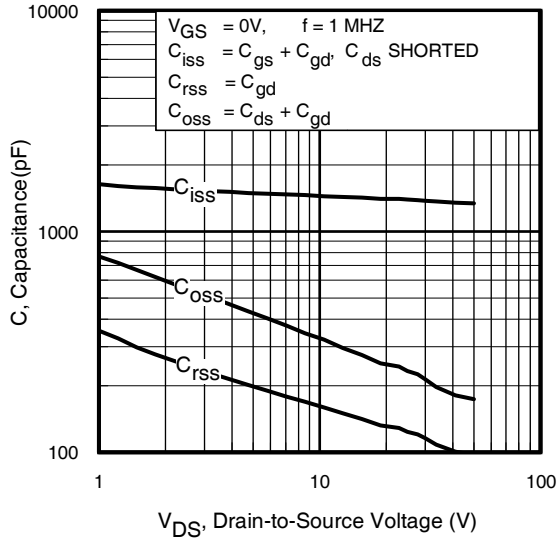
**Fig 2.** Typical Output Characteristics



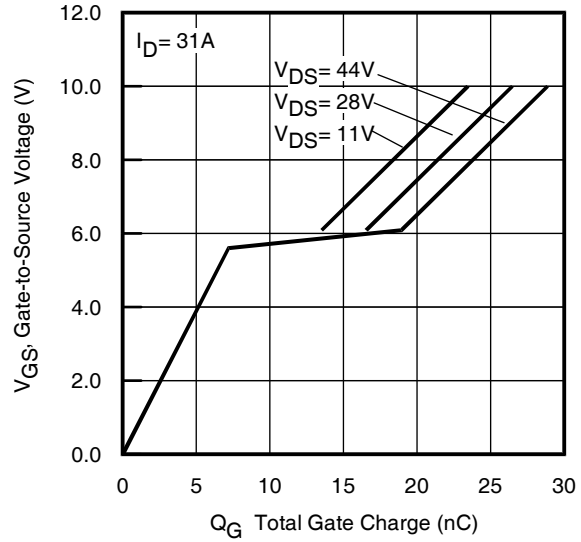
**Fig 3.** Typical Transfer Characteristics



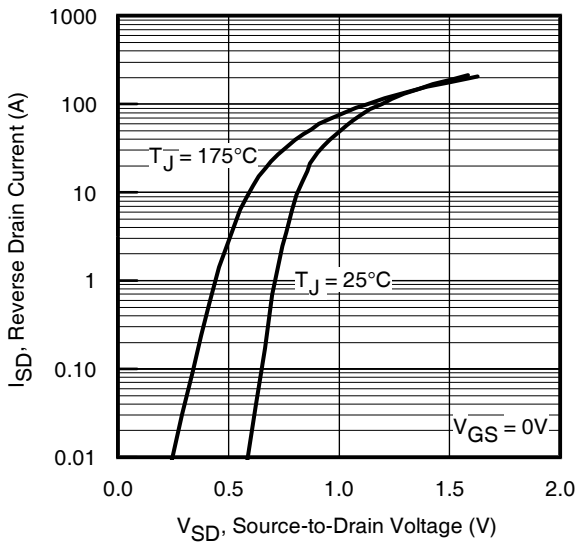
**Fig 4.** Typical Forward Transconductance vs. Drain Current



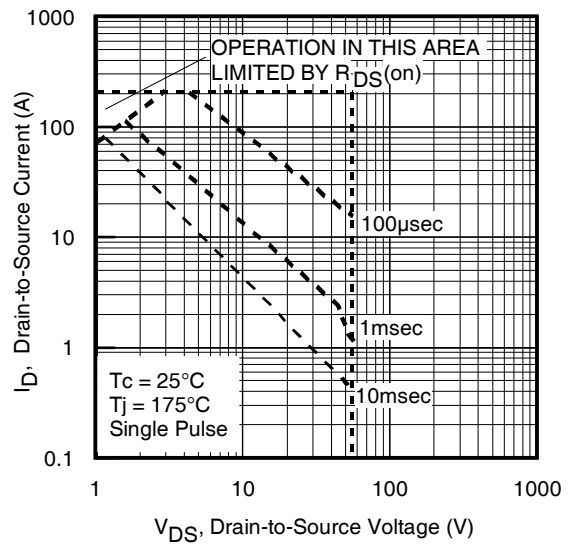
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



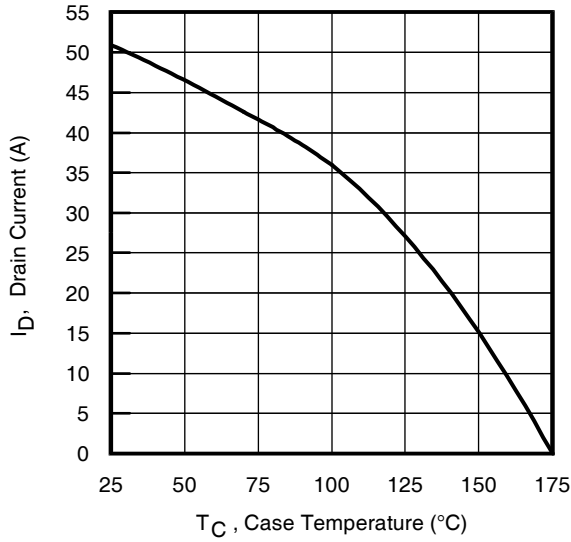
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



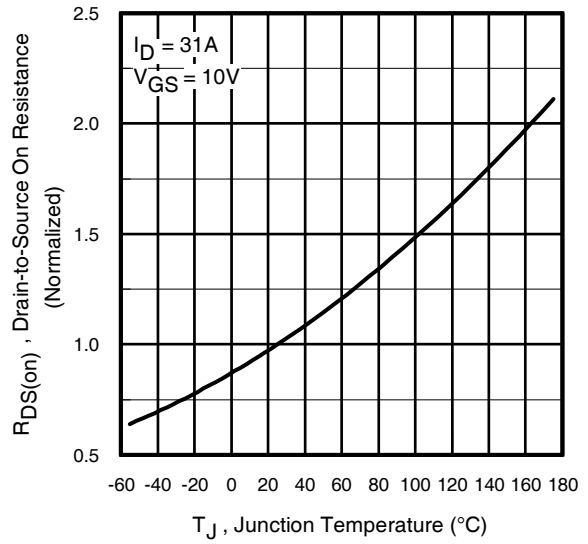
**Fig 7.** Typical Source-Drain Diode Forward Voltage



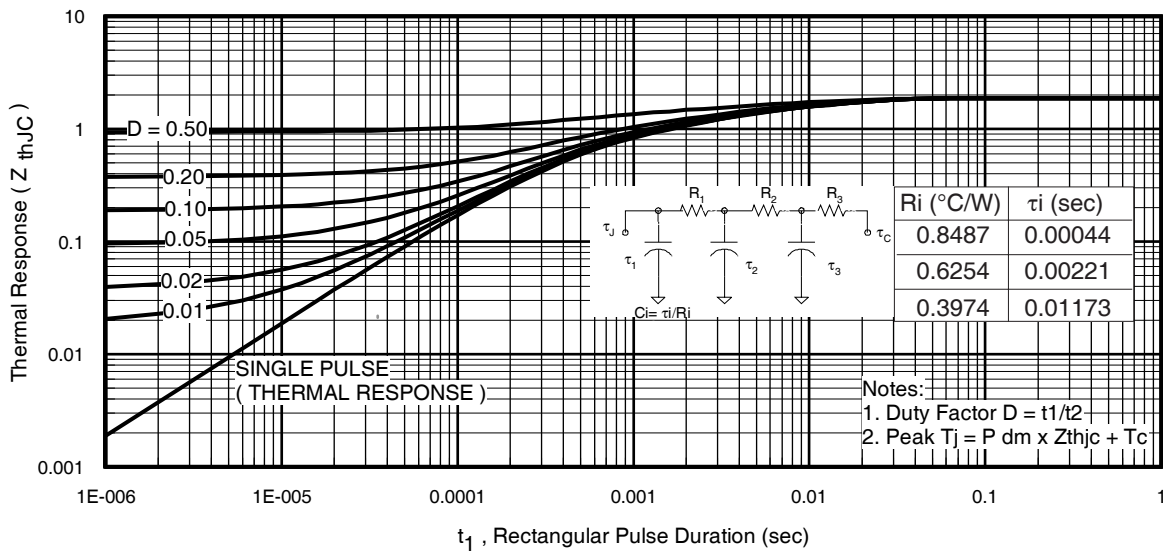
**Fig 8.** Maximum Safe Operating Area



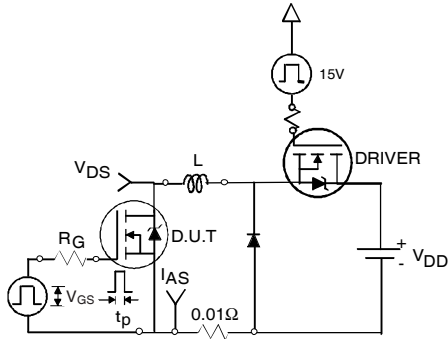
**Fig 9.** Maximum Drain Current vs. Case Temperature



**Fig 10.** Normalized On-Resistance vs. Temperature



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



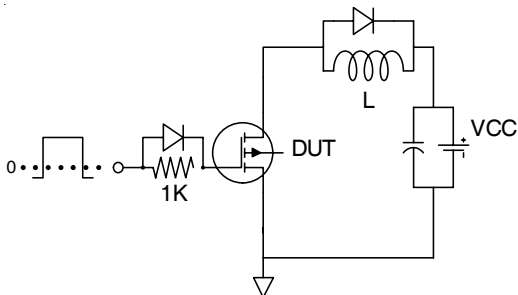
**Fig 12a.** Unclamped Inductive Test Circuit



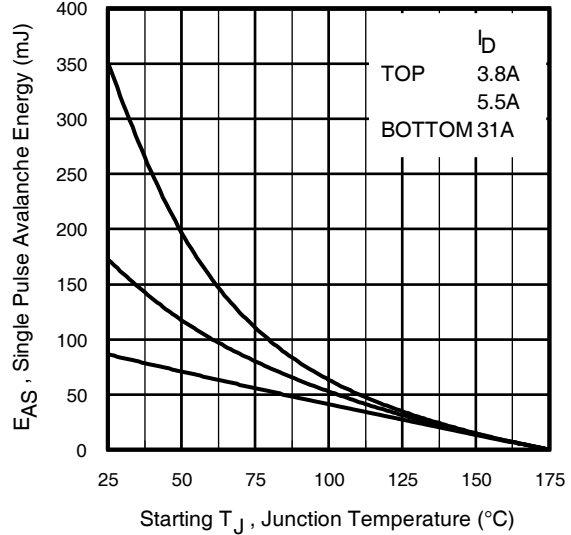
**Fig 12b.** Unclamped Inductive Waveforms



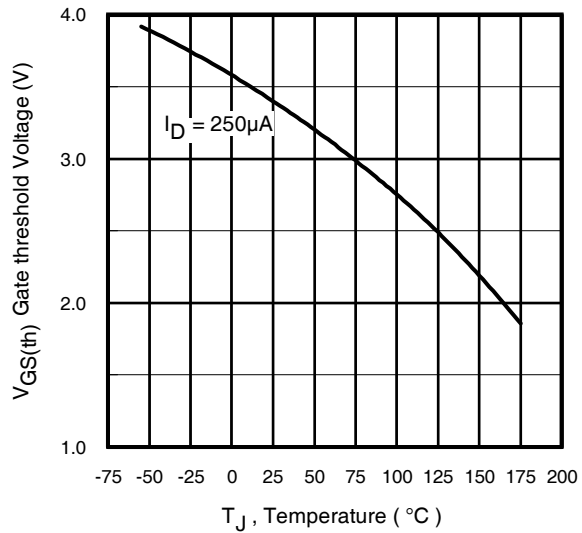
**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy vs. Drain Current



**Fig 14.** Threshold Voltage vs. Temperature

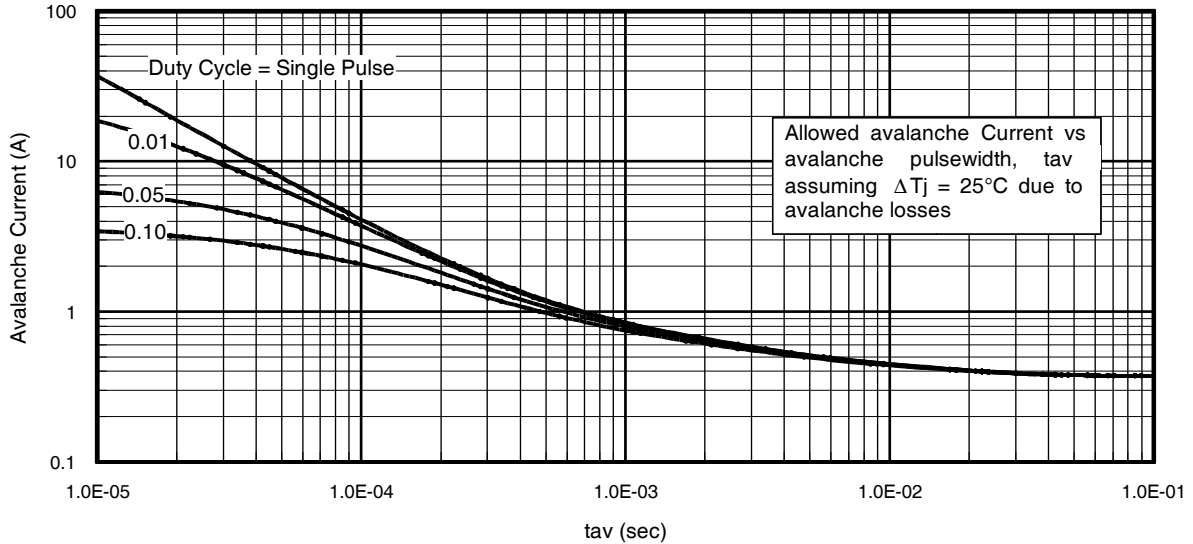


Fig 15. Typical Avalanche Current vs.Pulsewidth

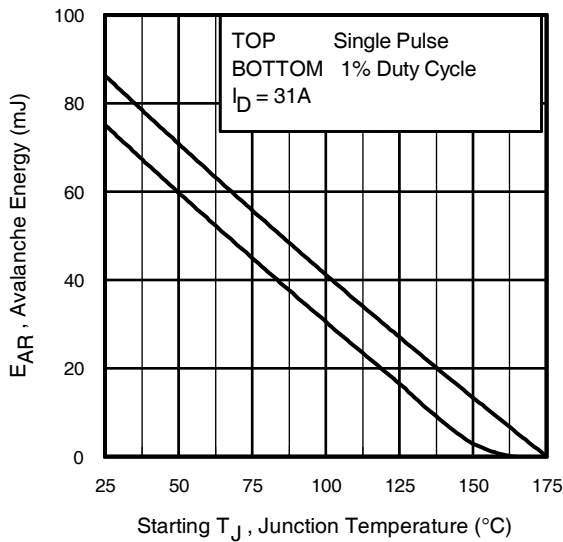


Fig 16. Maximum Avalanche Energy vs. Temperature

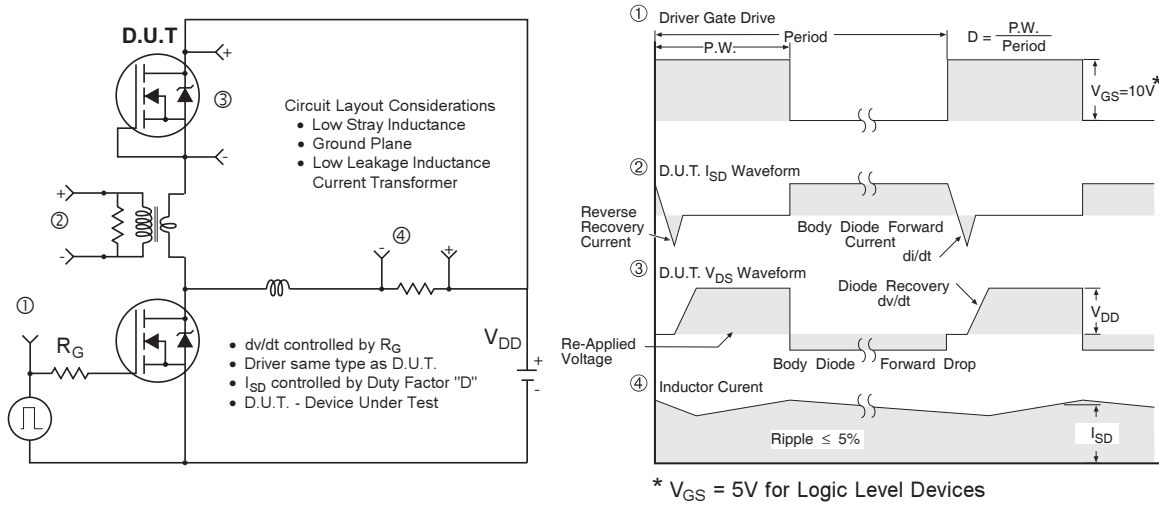
**Notes on Repetitive Avalanche Curves , Figures 15, 16:**  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

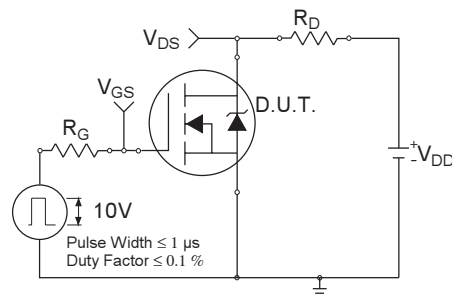
$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



**Fig 17. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**



**Fig 18a. Switching Time Test Circuit**

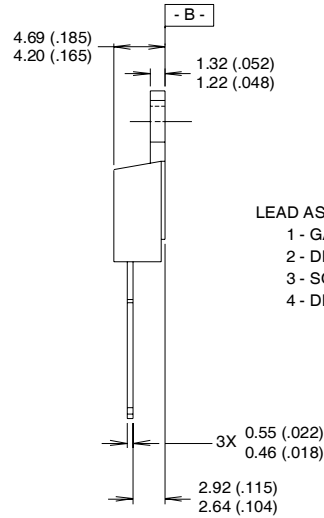
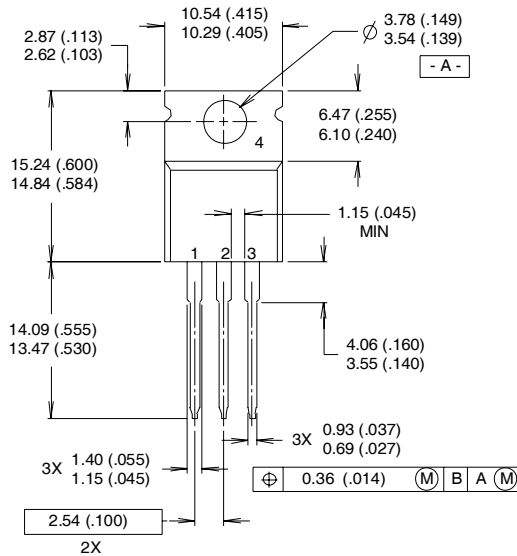


**Fig 18b. Switching Time Waveforms**



## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



### LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE
- 4 - DRAIN

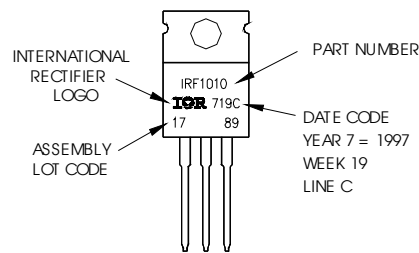
### NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH

- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

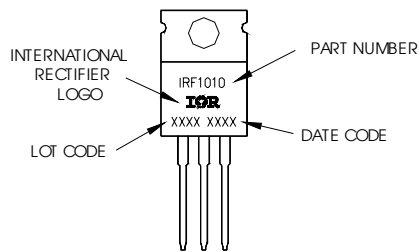
## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"



### For GB Production

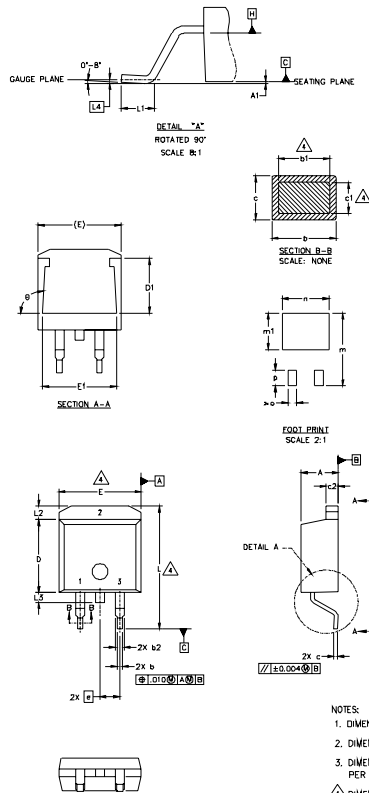
EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"



# IRFZ44Z/S/L

## D<sup>2</sup>Pak Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1		0.127		.005	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.43	0.63	.017	.025	
c1	0.38	0.74	.015	.029	
c2	1.14	1.40	.045	.055	3
D	8.51	9.65	.335	.380	
D1	5.33		.210		3
E	9.65	10.67	.380	.420	
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	
L2		1.65		.065	
L3	1.27	1.78	.050	.070	
L4	0.25 BSC		.010 BSC		
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
θ	90°	93°	90°	93°	

### LEAD ASSIGNMENTS

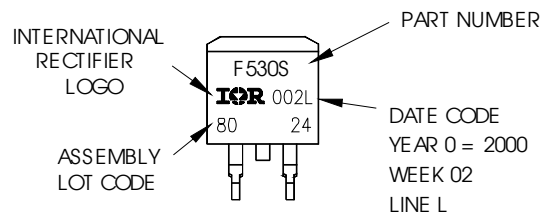
HEXFET	IGBTs, CoPACK	DIODES
1.- GATE	1.- GATE	1.- ANODE *
2.- DRAIN	2.- COLLECTOR	2.- CATHODE
3.- SOURCE	3.- EMITTER	3.- ANODE

\* PART DEPENDENT.

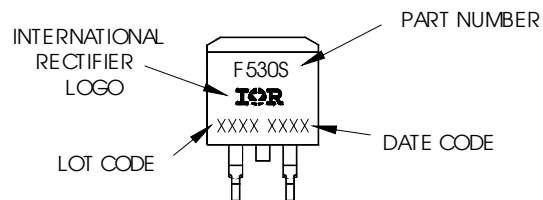
- NOTES:
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  - DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  - DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  - DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
  - CONTROLLING DIMENSION: INCH.

## D<sup>2</sup>Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON WW02, 2000  
IN THE ASSEMBLY LINE "L"

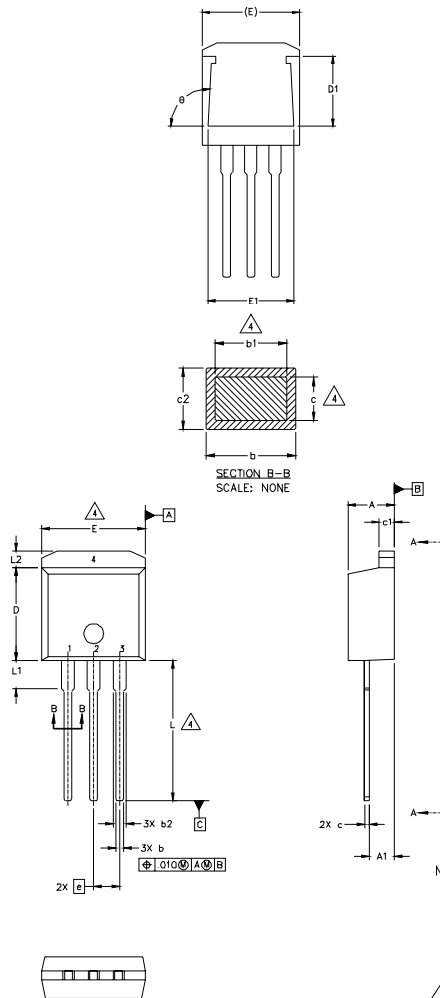


For GB Production  
EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON WW02, 2000  
IN THE ASSEMBLY LINE "L"



## TO-262 Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	4
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.38	0.63	.015	.025	4
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54	BSC	.100	BSC	
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

### LEAD ASSIGNMENTS

#### HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

#### IGBT

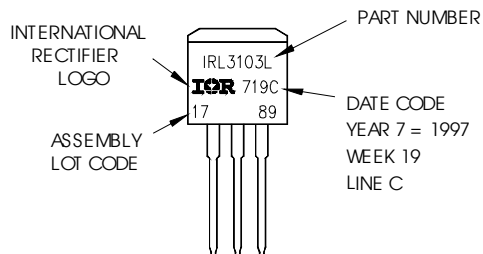
- 1- GATE
- 2- COLLECTOR
- 3- EMITTER

#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"

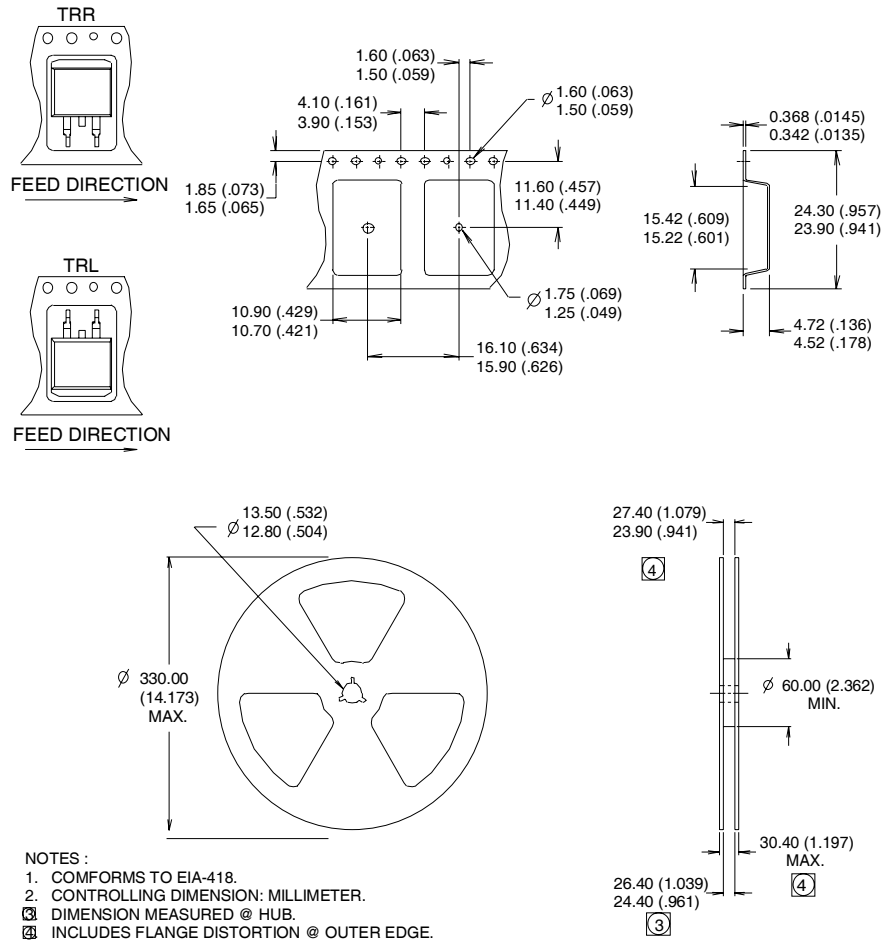


# IRFZ44Z/S/L

International  
**IR** Rectifier

## D<sup>2</sup>Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



**TO-220AB package is not recommended for Surface Mount Application.**

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Automotive [Q101] market.  
Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
TAC Fax: (310) 252-7903

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