Datasheet

APM32F030x6/x8

Arm® Cortex®-M0+ based 32-bit MCU

Version: V1.3

1. Product characteristics

- **System Architecture**
  - 32-bit Arm® Cortex®-M0+core
  - Up to 48MHz working frequency
- **Memories**
  - Flash: 32~64Kbytes
  - SRAM： 4~8Kbytes
- **Clock, reset and power management**
  - External supply voltage: V_{DD} =2.0~3.6V
  - Analog power supply: V_{DDA} = V_{DD} ~3.6V
  - Power-on/power-down reset (POR/PDR)
  - 4~32MHz crystal oscillator
  - RTC 32KHz oscillator with calibration
  - Internal 40 KHz RC oscillator
- **Low power consumption mode**
  - Sleep, halt and standby
- **Up to 55 fast I/O pins**
  - Supports all mappable external interrupt vectors
  - Almost all I/O pins are compatible with 5V input
- **5-channel DMA controller**
- **12-bit ADC**
  - Up to 16 external channels are supported
  - Conversion range: 0 ~ 3.6V.
  - Independent analog power supply: 2.4~3.6V
- **Real-time clock RTC**
  - Support calendar function
  - It can be used for alarm and periodic wake-up in halt and standby mode
- **10 timers**
  - 1 16-bit advanced control timer with 7-channel PWM output
  - Up to 5 general-purpose 16-bit timers
  - 1 16-bit basic timer
  - Independent watchdog and system window watchdog timer
  - System tick timer
- **communication interface**
  - Up to 2 I2C interfaces
  - Up to 2 USART interfaces
  - Up to 2 SPI interfaces
- **CRC calculation unit**
- **Serial wire debugging (SWD)**
- **96-bit UID**

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2. Brief introduction

The APM32F030x6/x8 series chips are 32-bit high-performance microcontrollers based on Arm® Cortex®-M0+core, and the working frequency can reach 48MHz. Built-in high-speed memory (up to 64 kbytes of flash memory and 8 kbytes of SRAM), the chip pins are multiplexed with a large number of enhanced peripherals and I/O. All chips provide standard communication interfaces: I2C interface, SPI interface and USART interface.

The working temperature range of APM32F030x6/x8 microcontroller is -40℃ ~+105℃, and the voltage range is 2.0~3.6V Many power-saving modes ensure the requirements of low-power applications.

The APM32F030x6/x8 microcontroller includes many different packages with 32, 48 and 64 pins, and different package forms make the peripheral configuration of the device different.

For information about the Arm® Cortex®-M0+core, please refer to the Arm® Cortex®-M0+technical reference manual, which can be downloaded from ARM's website.

3. Function description

See the following table for specific APM32F030x6/x8 product functions and peripheral configuration.

Table 1 **The functions and peripherals of APM32F030x6/x8 series chips**

Products		**APM32F030**					
Model		**K6U6**	**K6T6**	**K8T6**	**C6T6**	**C8T6**	**R8T6**
Encapsulation		**QFN32**	**LQFP32**	**LQFP32**	**LQFP48**	**LQFP48**	**LQFP64**
Flash memory (Kbytes)		32		64	32	64	
SRAM(Kbytes)		4		8	4	8	
Timer	16-bit universal	4(1)				5	
	16-bit advanced	1					
	Basic	-	-	-	-	1	
	24-bit down counter	1					
	Watchdog (WDT)	2					
	Real-time clock	1					
communication interface	USART	1(2)				2	
	SPI	1(3)				2	
	I2C	1(4)				2	
12-bit ADC	Unit	1					
	External channel	10					16
	Internal channel	2					
GPIOs		26			39		55
Maximum CPU frequency		M0+@48MHz					
Ambient temperature		Operating temperature: -40 c to 85°C /-40 c to 105°C Junction temperature: -40 C to 105°C /-40 C to 125°C					
Working voltage		2.0~3.6V					

Note:

(1) TMR15 does not exist.

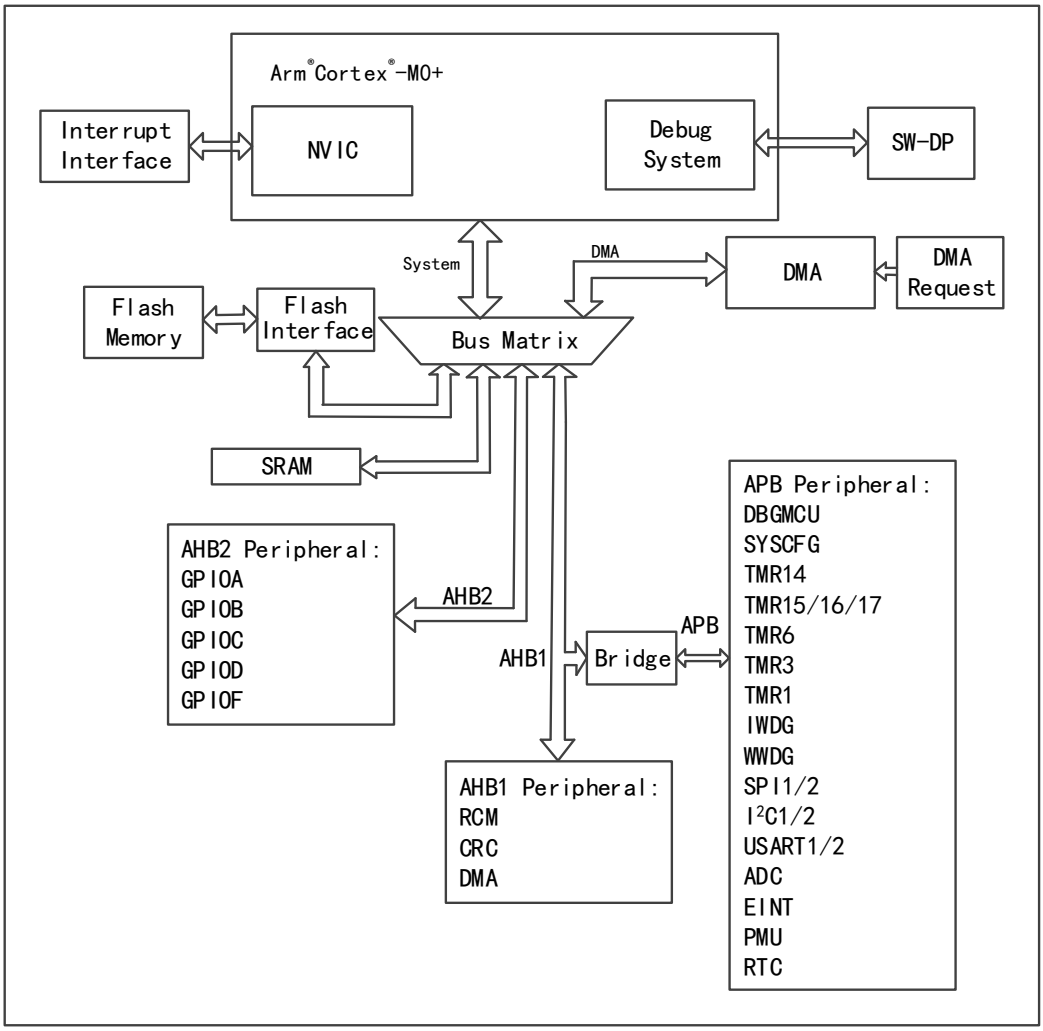
(2) USART2 does not exist.

(3) SPI2 does not exist.

(4) I2C2 does not exist.

3.1. System block diagram

Figure 1 System block diagram



3.2. Core

The Arm® Cortex®-M0+core is the latest generation of embedded Arm core. It is a low-cost platform, and APM32 is developed based on this platform, which has made a lot of optimization for system power consumption, while APM32 provides excellent computing performance and advanced system interrupt response.

The APM32F0xx series is based on the embedded ARM core, so it is compatible with all ARM tools and software.

The functional block diagram of APM32F030x6/x8 series products is shown in figure 1.

3.3. Memory

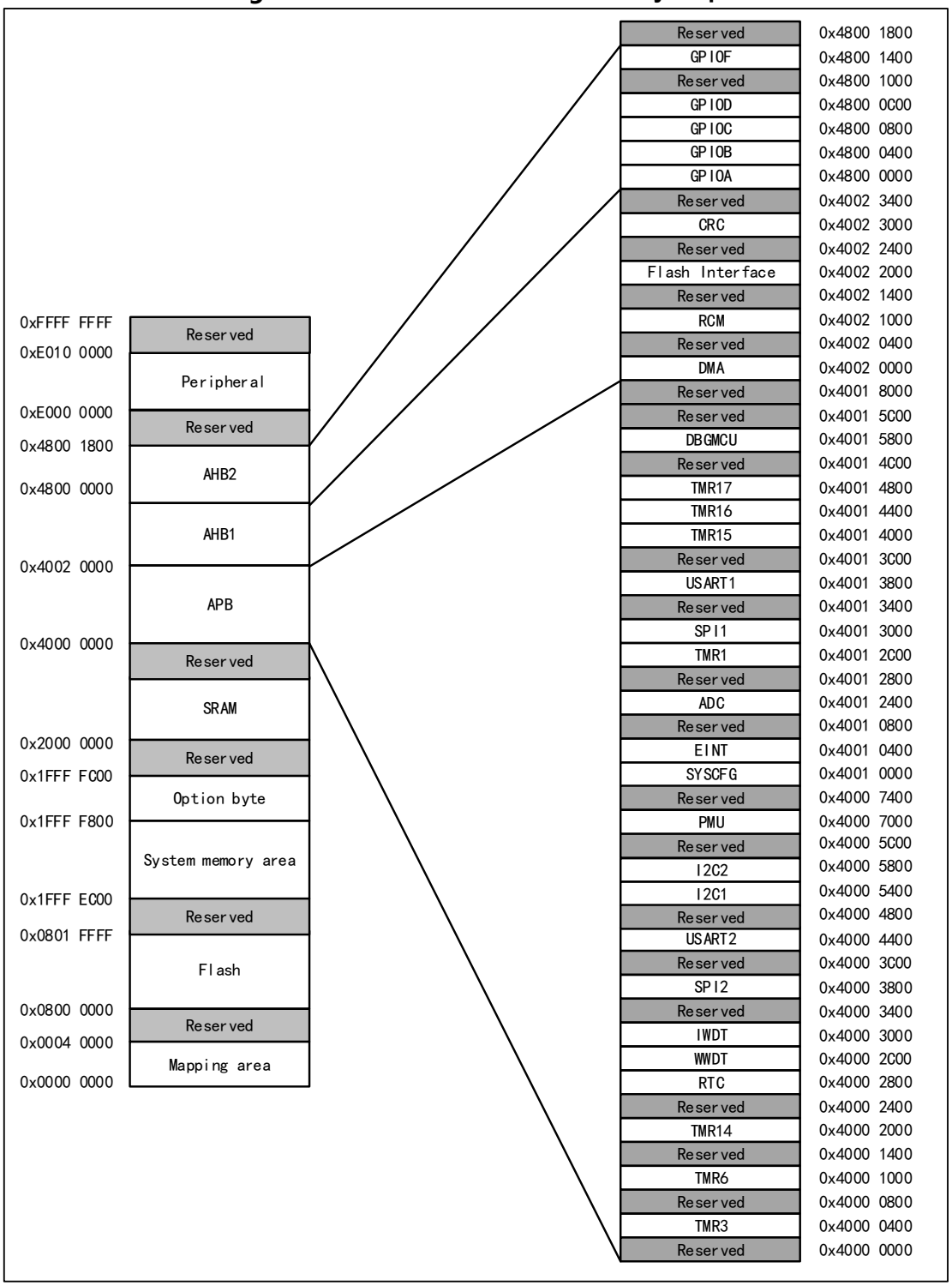
See the following table for memory details:

Table 2 **Memory description**

Memory	Max bytes	Function
Embedded flash memory	64Kbytes	Used to store programs and data
SRAM	8Kbytes	Used to store temporary data
Option byte	16bytes	Used to write protect memory and to protect the whole memory

3.4. Address mapping

Figure 2 APM32F030x6/x8 memory map



3.5. Power management

3.5.1 Power supply scheme

Table 3 **Power supply scheme**

Name	Voltage range	description
V_{DD}	2.0~3.6V	V_{DD} directly supplies power to IO port, and V_{DD} supplies power to core circuit through voltage regulator
V_{DDA}	V_{DD}~3.6V	V_{DDA} supplies power to ADC, reset module, RC oscillator and PLL. The V_{DDA} voltage level must always be greater than or equal to the V_{DD} voltage level, and it should be given priority

Note: See Figure 9 (Power Supply Scheme) for more details on how to connect power supply pins.

3.5.2 Voltage regulator

There are three main modes of voltage regulator. The working mode of MCU can be adjusted by voltage regulator to reduce power consumption. See the following table for details of the three modes.

Table 4 **Operation mode of voltage regulator**

Name	description
Master mode (MR)	Used in normal operation mode.
Low power mode (LPR)	It can be used in halt mode when power demand decreases.
Power-down mode	Used in power standby mode, the output of the voltage regulator is high impedance, the power supply of the core circuit is cut off, the voltage regulator is in zero consumption state, and all the data of registers and SRAM will be lost.

Note: The voltage regulator is always in working state after reset, and outputs with high impedance in power-down mode.

3.5.3 Power supply monitor

Two circuits of power-on reset (POR) and power-down reset (PDR), are integrated inside the product. These two circuits are always in working condition. When the power-down reset circuit monitors that the power supply voltage is lower than the specified threshold $V_{POR/PDR}$, the system enters the reset state, so it does not need to use an external reset circuit.

For details of $V_{POR/PDR}$, please refer to 5. Test Conditions, Low Power

Consumption Mode.

The APM32F0xx series supports the following three low power consumption modes, which can be configured by users to meet the best application requirements.

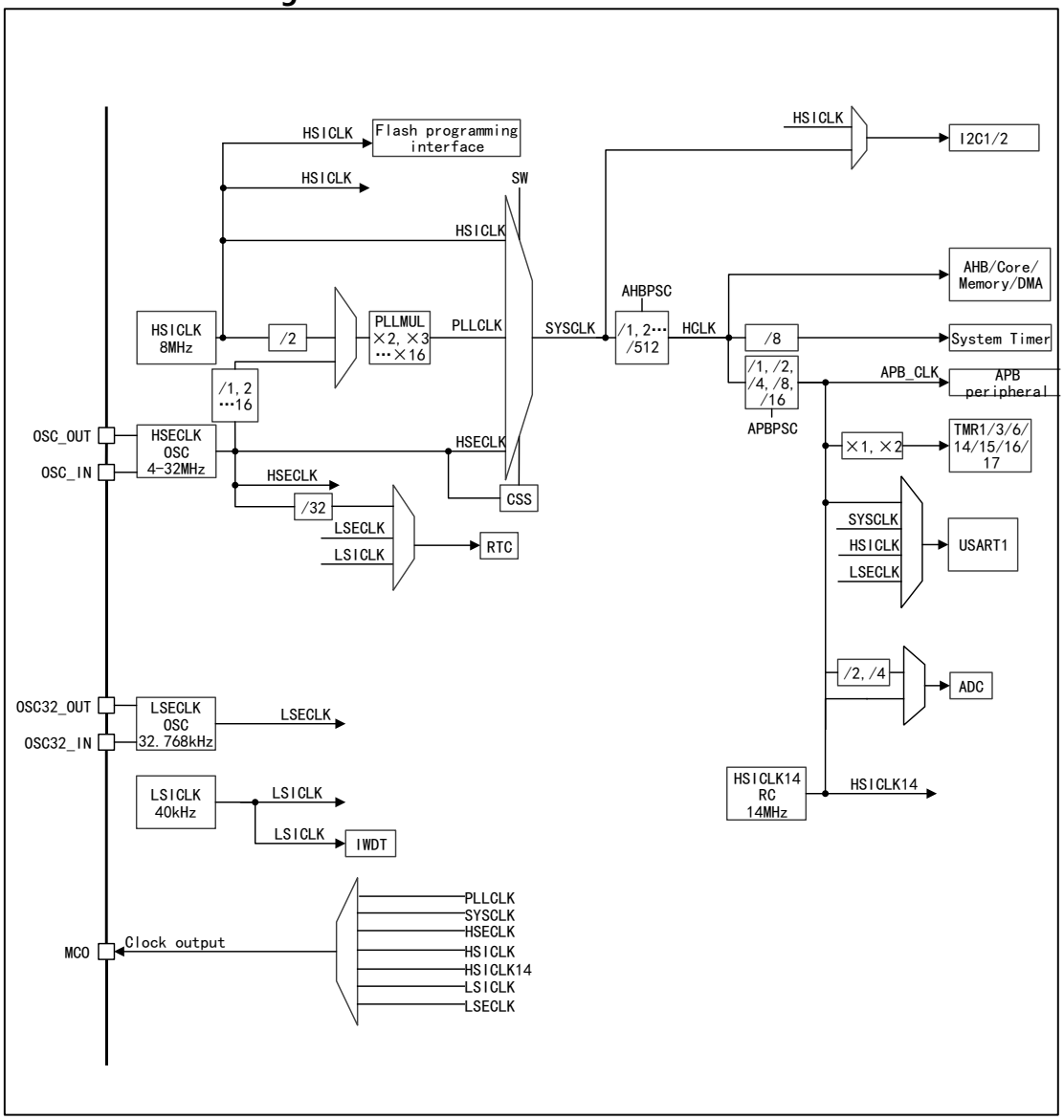
Table 5 **Low power consumption mode**

Mode type	description
Sleep mode	In sleep mode, the CPU stops working, all peripherals are in working state, and interrupts/events can wake up the CPU.
halt mode	halt mode can achieve the lowest power consumption mode without losing SRAM and register data. At this time, the internal 1.5V power supply is stopped, which causes the clocks of HSECLK, HSICLK and PLL to turn off, and the voltage regulator is placed in normal mode or low power consumption mode. Interrupt and event wake-up configured as EINT can wake up CPU from halt mode. EINT signal includes one of 16 external I/O ports, RTC alarm clock or USB wake-up signal.
Standby mode	Standby mode is the lowest power consumption mode used by the chip. At this time, the internal voltage regulator is turned off, which causes the power supply of the internal 1.5V part to be cut off, and the clocks of HSECLK, HSICLK and PLL are turned off; SRAM and register data will also disappear. However, the contents of the backup register remain, and the standby circuit still works. The external reset signal on NRST, IWDT reset, a rising edge on WKUP pin or RTC alarm clock will terminate the chip standby mode.

Note: RTC, IWDT and corresponding clocks still work normally in halt or standby mode.

3.6. Clock tree

Figure 3 Clock tree of APM32F030x6/x8



3.7. Clock and startup

Users can use 4~32MHz external high-speed clock with "failure monitoring" function through configuration. When the system clock does not detect that the external clock is configured, the system will automatically switch to the internal RC oscillator.

3.8. Real time clock (RTC)

RTC is an independent BCD timer/counter, which can not only support calendar function, but also have alarm clock interrupt and periodic interrupt function. Besides sub-second, second, minute, hour (12 or 24-hour format), week, date, month and year, the calendar clock existing in BCD (binary coded decimal system) format, the calendar function can also automatically adjust one month to 28, 29(leap year), 30 and 31 days.

Users can dynamically adjust RTC clock pulses from 1 to 32767. By adjusting RTC clock pulse to synchronize RTC and master clock, it can compensate the inaccuracy of quartz crystal, and the resolution of its digital calibration circuit is 1ppm. RTC has two programmable filter anti-tampering detection pins, which can wake up MCU in halt and standby modes when tampering events are detected. In addition, RTC has time stamp function, which can be used to save calendar contents. The timestamp function of RTC can be triggered by events on pins or tampering events. The MCU can wake up from the halt and standby modes when detecting a time event. The reference clock detection can use a more accurate second source clock (50 or 60Hz) to improve the accuracy of the calendar. Its clock source can be an external crystal oscillator, resonator or oscillator with 32.768kHz, an internal RC oscillator with low power consumption (typical frequency is 40KHz) or a high-speed external clock with 32 frequency division.

3.9. Startup mode

At startup, the user can select one of the following three startup modes by setting the high and low levels of the Boot pin:

- Startup from user Flash
- Startup from system memory
- Startup from embedded SRAM

Users can use USART to reprogram user Flash (ISP) when startup from system memory.

3.10. CRC calculation unit

A CRC (Cyclic Redundancy Check) calculation unit obtains a CRC code through a generator polynomial algorithm.

3.11. Interrupt controller

3.11.1 Nested Vector Interrupt Controller (NVIC)

The APM32F030x6/x8 product has a nested vector interrupt controller, and NVIC can handle up to 32 maskable interrupt channels (excluding 16 interrupt lines of Cortex®-M0+) and 4 priorities.

Nested Vector Interrupt Controller (NVIC) has a tightly coupled NVIC interface, which directly transmits the interrupt vector entry address to the kernel, thus achieving low-latency interrupt response processing. In addition, it can give priority to late arriving higher priority interrupts

3.11.2 External Interrupt/Event Controller (EINT)

The external interrupt/event controller consists of 32 edge detectors that generate event/interrupt requests. Its trigger events (rising edge or falling edge or double edge) can be independently configured or shielded; There is a register that holds the status of all interrupt requests. Up to 55 general-purpose I/OS can be connected to 16 external interrupt lines. EINT can detect pulses whose width is smaller than the internal clock period.

3.12. DMA

Five flexible general-purpose DMA can transfer data from memory to memory, from peripheral to memory and from memory to peripheral. The DMA controller supports the management of the ring buffer, and when the controller reaches the end of the buffer, there is no need for user code intervention.

Each channel has special hardware DMA request logic, and each channel can be triggered by software, and the address and target address can also be set independently by software.

DMA can be used for major peripherals: SPI, I2S, I2C, USART, all TMRx timers (except TMR14) and ADC.

3.13. Timer

The APM32F030x6/x8 product includes up to five general timers, a basic timer and an advanced control timer.

Table 6 **Advanced control timer**

Timer type	Advanced control timer
Timer	TMR1
Counter resolution	16 bits
Counter type	Up, down, up/down
Prescaler coefficient	Any integer between 1 and 65536
DMA request generation	Yes
Acquisition/comparison channel	4
Complementary output	Yes
Function description	It has complementary PWM output with dead band insertion, and can also be regarded as a complete general timer. When configured as a 16-bit standard timer, it has the same function as the TMRx timer. When configured as a 16-bit PWM generator, it has full modulation capability (0~100%). In debug mode, the timer can be frozen. Provides synchronization or event linking.

Table 7 **Basic timer**

Timer type	Basic timer
Timer	TMR6
Counter resolution	16 bits
Counter type	Up
Prescaler coefficient	Any integer between 1 and 65536
DMA request generation	Yes
Acquisition/comparison channel	0
Complementary output	-
Function description	It can be used as a universal 16-bit time base clock

Table 8 **General timer**

Timer type	**General timer**				
Timer	TMR3	TMR14	TMR15	TMR16	TMR17
Counter resolution	16 bits	16 bits	16 bits	16 bits	
Counter type	Up, down, Up, down	Up	Up	Up	
Prescaler	Any integer between 1 and 65536	Any integer between 1 and 65536	Any integer between 1 and 65536	Any integer between 1 and 65536	
DMA request generation	Yes	No	Yes	Yes	
Capture/ Comparison Channels	4	1	2	1	
Function description	There are 4 independent channels, each for input capture/output comparison, PWM or single pulse mode output. Up to 12 input capture, output comparison or PWM channels can be provided in the largest package configuration. It has an independent DMA request generation.	Single channel, PWM or single pulse mode output function for input capture/output comparison.	It has complementary output function with dead zone generation and independent DMA request generation. These three timers can work together, and TMR15 operates with TMR1 through link function, which can realize synchronization or event link function. TMR15 has two independent channels, while TMR16 and TMR17 are synchronized. TMR15 can be synchronized with TMR16 and TMR17.		

Table 9 **Comparison between independent watchdog and window watchdog**

Name	**Counter Resolution**	**Counter type**	**Prescaler coefficient**	**Function description**
Independent watchdog (IWDT)	12 bits	down	Between 1 and 256 Arbitrary integer	The clock is provided by an internally independent RC oscillator of 40KHz, which is independent of the master clock, so it can run in halt and standby modes. The whole system can be reset in case of problems. You can provide timeout management for applications. It can be configured as a software or hardware startup watchdog.

Name	Counter Resolution	Counter type	Prescaler coefficient	Function description
				In debug mode, the counter can be paused for convenience of debugging.
Window watchdog (WWDT)	7 bits	down	-	It can be set to run freely. The whole system can be reset in case of problems. Driven by the master clock, it has early interrupt warning function. Timers in debug mode can be frozen.

3.14. System tick timer

System tick timer is a standard 24-bit down counter with automatic reloading function. When the counter is 0, it can generate a masked system interrupt and can program the clock source (HCLK or HCLK/8).

3.15. communication interface

3.15.1 I2C bus

I2C1/2 can work in master mode and slave mode, and supports 7-bit and 10-bit addressing modes. I2C1/2 supports standard mode (up to 100kbit/s) or fast mode (up to 400kbit/s). In addition, I2C1 has built-in programmable analog and digital noise filters, and also supports ultra-fast mode (up to 1 Mbit/s).

In addition, I2C1 also provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP function, host notification protocol, hardware CRC(PEC) generation/verification, timeout verification and alarm protocol management.

I2C supports DMA function.

See table 10 for the differences between I2C1 and I2C2.

Table 10 **APM32F030x6/x8I2C function**

I2C function	I2C1	I2C2 (2)
7-bit addressing mode	√ (1)	√
10-bit addressing mode	√	√
Standard mode (up to 100kbit/s)	√	√
Fast mode (up to 400kbit/s)	√	√
Ultra-fast mode (up to 1Mbit/s), I/O port supports 20mA output current drive	√	-

I2C function	I2C1	I2C2 (2)
Independent clock	√	-
SM bus	√	-
Wake up from halt	-	-

Note:

(1) √ = support

(2) Available only on APM32F030x8 chip.

3.15.2 Universal synchronous/asynchronous transceiver (USART)

Up to two universal synchronous/asynchronous transceivers are built in the chip, and the communication rate can reach 6Mbit/s at the highest. All USART interfaces can be provided by DMA controller, and the functions that USART interfaces can realize are shown in the following table.

Table 11 **APM32F0x6/8 USART function**

USART mode/function	APM32F030x6	APM32F030x8	
	USART1	USART1	USART2
Hardware flow control of modem	√	√	√
Continuous communication using DMA	√	√	√
Multiprocessor communication	√	√	√
Synchronization mode	√	√	√
Smart card mode	-	-	-
Single wire half duplex communication	√	√	√
IrDA SIR codec module	-	-	-
LIN mode	-	-	-
Dual clock domain and wake-up from halt mode	-	-	-
Receiver timeout interrupt	√	√	-
MODBUS communication	-	-	-
Auto baud rate detection (supported mode)	2	2	-
USART data length	8 bits and 9 bits		

Note: √ = support.

3.15.3 Serial peripheral interface (SPI)

Two SPI interfaces are embedded in APM32F0xx series, which enables the chip to communicate with external devices in half/full duplex serial mode. The interface can be configured as master mode or slave mode. Eight master mode frequencies can be generated by a 3-bit prescaler, with 4~16 bits per frame and

a communication rate of 18 Mbit/s.

The functions of SPI1 and SPI2 are similar, see the table below for details.

Table 12 **APM32F030x6/x8 SPI function**

SPI function	SPI	SPI2(2)
Calculation of hardware cyclic redundancy check	√ (1)	√
Receive/Send first in first out (FIFO)	√	√
NSS pulse mode	√	√
TI mode	√	√

Note:

(1) √ = supported.

(2) Available only on APM32F030x8 chip.

3.16. General purpose input/output interface (GPIO)

Each GPIO pin can be configured as an output (push-pull or open drain), an input (with or without pull-down) or a multiplexed peripheral function port by software. Most GPIO pins can be shared with digital or analog multiplexed peripherals.

The peripheral functions of I/O pins can be locked by a specific operation sequence to avoid accidental writing to I/O registers.

3.17. ADC (analog/digital converter)

The 12-bit A/D converter has up to 16 external channels and 2 internal channels (temperature sensor, voltage reference), which can perform single or scanning conversion.

The analog watchdog function can monitor multiple channels very accurately, and when the monitored signal exceeds the threshold value, an interrupt will be generated.

ADC supports DMA function.

3.17.1 Internal reference voltage (V_{REFINT})

The internal reference voltage (V_{REFINT}) provides a stable (band gap) voltage output for the ADC. V_{REFINT} is internally connected to the ADC_IN17 input channel.

Table 13 **Internal reference voltage calibration value**

Calibration value name	description	Memory address
VREFINT_CAL	Original data collected at 30°C(± 5 °C) and V_{DDA} = 3.3v (10mv)	0x1FFF F7BA - 0x1FFF F7BB

3.17.2 Serial wire debug port (SW-DP)

The product provides ARM SW-DP interface, through which MCU can be connected with serial line debugging tool.

4. Pin characteristics

4.1. Pin definition

Figure 4 Pin definition diagram of APM32F030x6/x8 series LQFP64

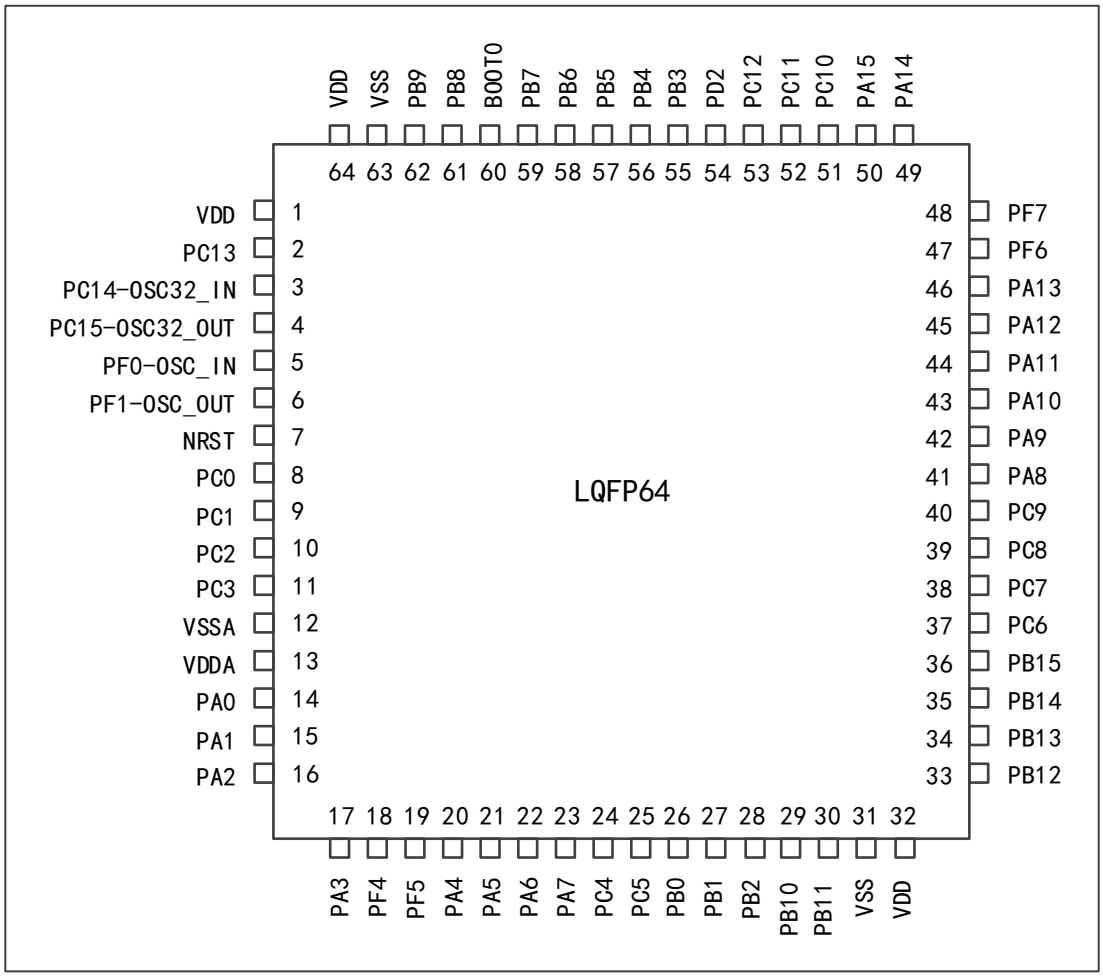


Figure 5 Pin configuration diagram of APM32F030x6/x8 series LQFP48

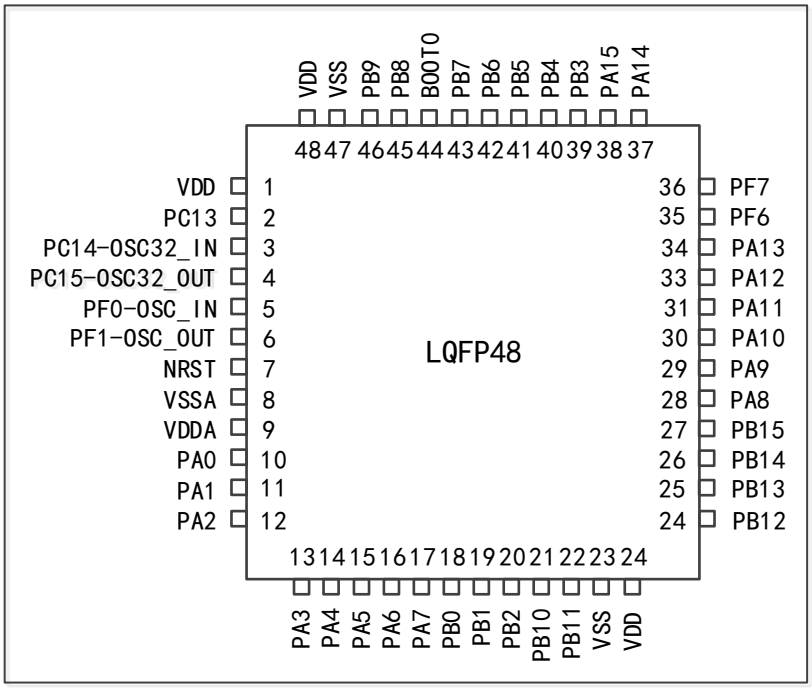


Figure 6 Pin configuration diagram of APM32F030x6/x8 series LQFP32

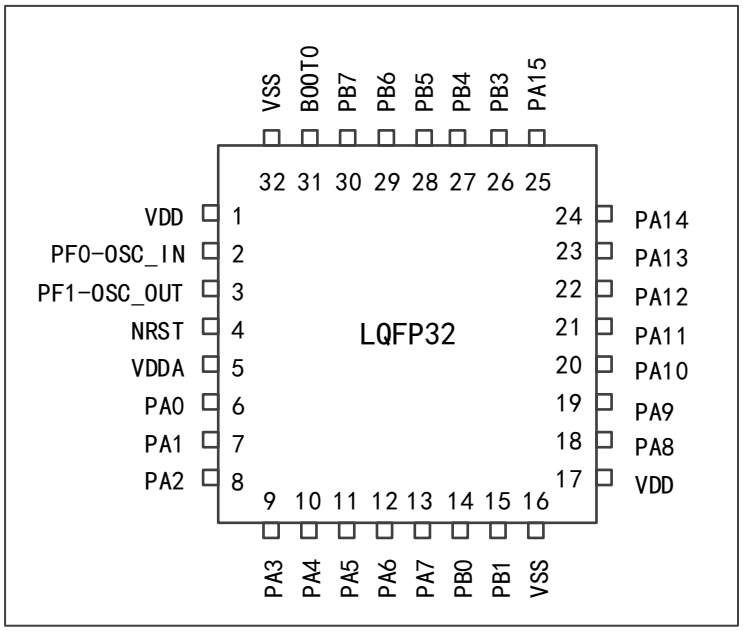
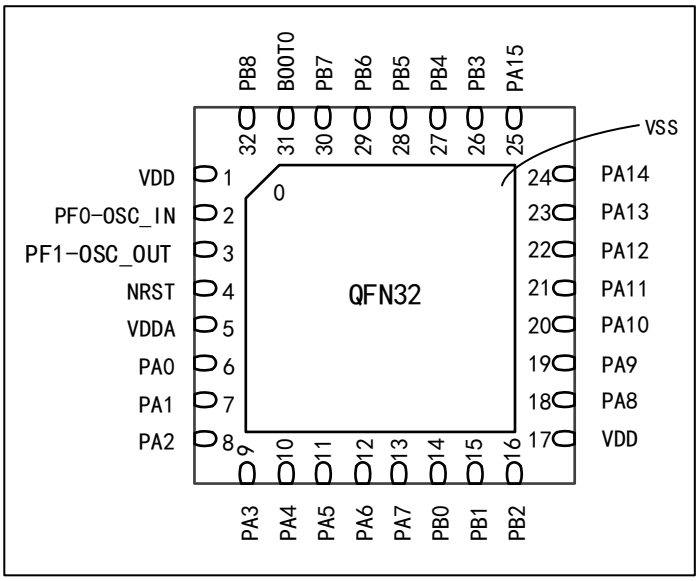


Figure 7 Pin configuration diagram of APM32F030x6/x8 series QFN32



4.2. Pin function description

Table 14 **Legend/abbreviation used in output pin table**

Name		Abbreviations	Definition
Pin name		Unless otherwise specified in parentheses below the pin name, the pin functions during and after reset are the same as the actual pin name	
Pin type		S	Power supply pin
		I	Input pins only
		I/O	I/O pins
I/O structure		FT	I/O with 5V tolerance
		FTf	I/O with 5 V tolerance, FM+ function
		TTa	I/O with 3.3 V tolerance is directly connected to ADC
		TC	Standard 3.3VI/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with built-in weak pull-up resistor
pay attention to		Unless otherwise specified in the notes, all I/O is set as floating input during and after reset	
Pin function	Multiplexing function	The function selected by GPIOx_AFR register	
	Additional function	Functions directly selected/enabled through peripheral registers	

Table 15 **Functional description of APM32F030x6/x8 pin**

Pin name (Function after reset)	Pin coding				Pin Type	I/O Structure	Notes	Pin function	
	LQFP64	LQFP48	LQFP32	QFN32				Multiplexing function	Additional function
V_{DD}	1	1	-	-	S	-	-	Complementary power supply	
PC13	2	2	-	-	I/O	TC	(1)	-	RTC_TAMP1, RTC_TS, RTC_OUT, WKUP2
PC14-OSC32_IN (PC14)	3	3	-	-	I/O	TC	(1)	-	OSC32_IN
PC15-OSC32_OUT (PC15)	4	4	-	-	I/O	TC	(1)	-	OSC32_OUT
PF0-OSC_IN (PF0)	5	5	2	2	I/O	FT	-		OSC_IN
PF1-OSC_OUT (PF1)	6	6	3	3	I/O	FT	-	-	OSC_OUT
NRST	7	7	4	4	I/O	RST	-	Chip reset input/internal reset output (active low)	
PC0	8	-	-	-	I/O	TTa	-	USART2_CTS	ADC_IN0, RTC_TAMP2, WKUP1
PC1	9	-	-	-	I/O	TTa	-	USART2_RTS, EVENTOUT	ADC_IN1
PC2	10	-	-	-	I/O	TTa	-	USART2_TX, TMR15_CH1	ADC_IN2
PC3	11	-	-	-	I/O	TTa	-	USART2_RX, TMR15_CH2	ADC_IN3
V_{SSA}	12	8	-	0	S	-	-	EVENTOUT	-
V_{DDA}	13	9	5	5	S	-	-	EVENTOUT	-
PA0	14	10	6	6	I/O	TTa	-	SPI1_NSS, USART2_CK, TMR14_CH1	ADC_IN4
PA1	15	11	7	7	I/O	TTa	-	SPI1_SCK	ADC_IN5
PA2	16	12	8	8	I/O	TTa	-	SPI1_MISO, TMR3_CH1, TMR1_BKIN, TMR16_CH1, EVENTOUT	ADC_IN6

Pin name (Function after reset)	Pin coding				Pin Type	I/O Structure	Notes	Pin function	
	LQFP 64	LQFP 48	LQFP 32	QFN 32				Multiplexing function	Additional function
PA3	17	13	9	9	I/O	TTa	-	SPI1_MOSI, TMR3_CH2, TMR14_CH1, TMR1_CH1N, TMR17_CH1, EVENTOUT	ADC_IN7
PF4	18	-	-	-	I/O	FT	-	EVENTOUT	ADC_IN14
PF5	19	-	-	-	I/O	FT	-	-	ADC_IN15
PA4	20	14	10	10	I/O	TTa	-	TMR3_CH3, TMR1_CH2N, EVENTOUT	ADC_IN8
PA5	21	15	11	11	I/O	TTa	-	TMR3_CH4, TMR14_CH1, TMR1_CH3N	ADC_IN9
PA6	22	16	12	12	I/O	TTa	-	-	-
PA7	23	17	13	13	I/O	TTa	-	I2C2_SCL	-
PC4	24	-	-	-	I/O	TTa	-	I2C2_SDA, EVENTOUT	-
PC5	25	-	-	-	I/O	TTa	-	USART2_CTS	ADC_IN0, RTC_TAMP2, WKUP1
PB0	26	18	14	14	I/O	TTa	-	USART2_RTS, EVENTOUT	ADC_IN1
PB1	27	19	15	15	I/O	TTa	-	USART2_TX, TMR15_CH1	ADC_IN2
PB2	28	20	-	16	I/O	FT	-	USART2_RX, TMR15_CH2	ADC_IN3
PB10	29	21	-	-	I/O	FT	-	EVENTOUT	-
PB11	30	22	-	-	I/O	FT	-	EVENTOUT	-
V_{SS}	31	23	16	0	S	-	-	ground	
V_{DD}	32	24	17	17	S	-	-	Digital power supply	
PB12	33	25	-	-	I/O	FT	-	SPI2_NSS, TMR1_BKIN, EVENTOUT	-
PB13	34	26	-	-	I/O	FT	-	SPI2_SCK, TMR1_CH1N	-
PB14	35	27	-	-	I/O	FT	-	SPI2_MISO, TMR1_CH2N, TMR15_CH1	-

Pin name (Function after reset)	Pin coding				Pin Type	I/O Structure	Notes	Pin function	
	LQFP64	LQFP48	LQFP32	QFN32				Multiplexing function	Additional function
PB15	36	28	-	-	I/O	FT	-	SPI2_MOSI, TMR1_CH3N, TMR15_CH1N, TMR15_CH2	RTC_REFIN
PC6	37	-	-	-	I/O	FT	-	TMR3_CH1	-
PC7	38	-	-	-	I/O	FT	-	TMR3_CH2	-
PC8	39	-	-	-	I/O	FT	-	TMR3_CH3	-
PC9	40	-	-	-	I/O	FT	-	TMR3_CH4	-
PA8	41	29	18	18	I/O	FT	-	USART1_CK, TMR1_CH1, EVENTOUT, MCO	-
PA9	42	30	19	19	I/O	FT	-	USART1_TX, TMR1_CH2, TMR15_BKIN	-
PA10	43	31	20	20	I/O	FT	-	USART1_RX, TMR1_CH3, TMR17_BKIN	-
PA11	44	32	21	21	I/O	FT	-	USART1_CTS, TMR1_CH4, EVENTOUT	-
PA12	45	33	22	22	I/O	FT	-	USART1_RTS, TMR1_ETR, EVENTOUT	-
PA13 (SWDIO)	46	34	23	23	I/O	FT	(2)	IR_OUT,SWDIO	-
PF6	47	35	-	-	I/O	FT		I2C2_SCL	-
PF7	48	36	-	-	I/O	FT		I2C2_SDA	-
PA14 (SWCLK)	49	37	24	24	I/O	FT	(2)	USART2_TX, SWCLK	-
PA15	50	38	25	25	I/O	FT	-	SPI1_NSS, USART2_RX, EVENTOUT	-
PC10	51	-	-	-	I/O	FT	-	-	-
PC11	52	-	-	-	I/O	FT	-	-	-
PC12	53	-	-	-	I/O	FT	-	-	-
PD2	54	-	-	-	I/O	FT	-	TMR3_ETR	-
PB3	55	39	26	26	I/O	FT	-	SPI1_SCK, EVENTOUT	-

Pin name (Function after reset)	Pin coding				Pin Type	I/O Structure	Notes	Pin function	
	LQFP64	LQFP48	LQFP32	QFN32				Multiplexing function	Additional function
PB4	56	40	27	27	I/O	FT	-	SPI1_MISO, TMR3_CH1, EVENTOUT	-
PB5	57	41	28	28	I/O	FT	-	SPI1_MOSI, I2C1_SMBA, TMR16_BKIN, TMR3_CH2	
PB6	58	42	29	29	I/O	FT	-	I2C1_SCL, USART1_TX, TMR16_CH1N	-
PB7	59	43	30	30	I/O	FT	-	I2C1_SDA, USART1_RX, TMR17_CH1N	-
BOOT0	60	44	31	31	I	B	-	Memory startup selection	
PB8	61	45	-	32	I/O	FTf	-	I2C1_SCL, TMR16_CH1	-
PB9	62	46	-	-	I/O	FTf	-	I2C1_SDA, IR_OUT, TMR17_CH1, EVENTOUT	-
V_{SS}	63	47	32	0	S	-	-	ground	
V_{DD}	64	48	1	1	S	-	-	Digital power supply	

Note:

(1) PC13, PC14 and PC15 are powered by the power switch. Because the switch only absorbs limited current (3 mA), the use of PC13 to PC15 of GPIO is limited in output mode: when the large load is 30 pF, the speed should not exceed 2 MHz; It is not used as a current source (for example, driving light emitting diodes).

(2) Upon reset, these pins are configured as SWDIO and SWCLK multiplexing functions, and the internal pull-up of SWDIO pin and the internal pull-down of SWCLK pin are activated.

Table 16 **Select multiplexing function for port A through GPIOA_AFR register**

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PA0	-	USART2_CTS	-	-		-	-
PA1	EVENTOUT	USART2_RTS	-	-			-
PA2	TMR15_CH1	USART2_TX	-	-	-	-	-
PA3	TMR15_CH2	USART2_RX	-	-	-	-	-
PA4	SPI1_NSS	USART2_CK	-	-	TMR14_CH1		-
PA5	SPI1_SCK	-	-	-	-		-
PA6	SPI1_MISO	TMR3_CH1	TMR1_BKIN	-		TMR16_CH1	EVENTOUT
PA7	SPI1_MOSI	TMR3_CH2	TMR1_CH1N	-	TMR14_CH1	TMR17_CH1	EVENTOUT
PA8	MCO	USART1_CK	TMR1_CH1	EVENTOUT	-	-	-
PA9	TMR15_BKIN	USART1_TX	TMR1_CH2	-			-
PA10	TMR17_BKIN	USART1_RX	TMR1_CH3	-		-	-
PA11	EVENTOUT	USART1_CTS	TMR1_CH4	-	-	SCL	-
PA12	EVENTOUT	USART1_RTS	TMR1_ETR	-	-	SDA	-
PA13	SWDIO	IR_OUT	-	-	-	-	-
PA14	SWCLK	USART2_TX	-	-	-	-	-
PA15	SPI1_NSS	USART2_RX	-	EVENTOUT		-	-

Table 17 **Select multiplexing function for port B through GPIOB_AFR register**

Pin name	AF0	AF1	AF2	AF3	AF4	AF5
PB0	EVENTOUT	TMR3_CH3	TMR1_CH2N	-		-
PB1	TMR14_CH1	TMR3_CH4	TMR1_CH3N	-		-
PB2	-	-	-	-	-	-
PB3	SPI1_SCK	EVENTOUT	-	-		-
PB4	SPI1_MISO	TMR3_CH1	EVENTOUT	-		TMR17_BKIN
PB5	SPI1_MOSI	TMR3_CH2	TMR16_BKIN	-		-
PB6	USART1_TX	I2C1_SCL	TMR16_CH1N	-	-	-
PB7	USART1_RX	I2C1_SDA	TMR17_CH1N	-		-
PB8	-	I2C1_SCL	TMR16_CH1	-	-	-
PB9	IR_OUT	I2C1_SDA	TMR17_CH1	EVENTOUT	-	-
PB10	-	I2C2_SCL	-	-		-
PB11	EVENTOUT	I2C2_SDA	-	-		-
PB12	SPI2_NSS	EVENTOUT	TMR1_BKIN	-		-
PB13	SPI2_SCK	-	TMR1_CH1N	-		
PB14	SPI2_MISO	TMR15_CH1	TMR1_CH2N	-		
PB15	SPI2_MOSI	TMR15_CH2	TMR1_CH3N	TMR15_CH1N	-	-

Table 18 **Select multiplexing function for port C through GPIOC_AFR register**

Pin name	AF0
PC0	EVENTOUT
PC1	EVENTOUT
PC2	EVENTOUT
PC3	EVENTOUT
PC4	EVENTOUT
PC5	-
PC6	TMR3_CH1
PC7	TMR3_CH2
PC8	TMR3_CH3
PC9	TMR3_CH4
PC10	
PC11	
PC12	
PC13	-
PC14	-
PC15	-

Table 19 **Select multiplexing function for port D through GPIOD_AFR register**

Pin name	AF0
PD2	TMR3_ETR

Table 20 **Select multiplexing function for port F through GPIOF_AFR register**

Pin name	AF0
PF0	-
PF1	-

5. Electrical specification

5.1. Test condition

All voltage parameters (unless otherwise specified) refer to V_{SS}.

5.1.1 Maximum and minimum value

Unless otherwise specified, all products are tested on the production line at T_A=25°C. Its maximum and minimum values can support the worst environmental temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data obtained through comprehensive evaluation, design simulation or process characteristics are not tested on the production line; On the basis of comprehensive evaluation, after passing the sample test, take the average value and add and subtract three times the standard deviation (average ±3∑) to get the maximum and minimum values.

5.1.2 Typical value

Unless otherwise specified, typical data are based on T_A=25°C and V_{DD}= V_{DDA}=3.3V; These data are for design guidance only.

5.1.3 Typical curve

Unless otherwise specified, typical curves will not be tested on the production line, and will only be used for design guidance.

5.1.4 Load capacitance

Figure 8 Load conditions when measuring pin parameters

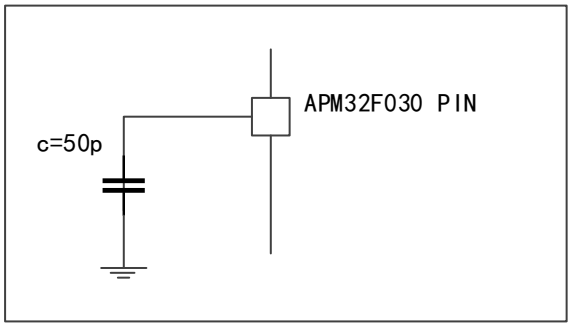


Figure 9 Pin input voltage measurement scheme

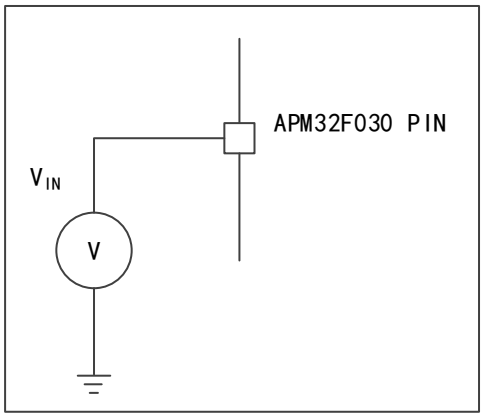
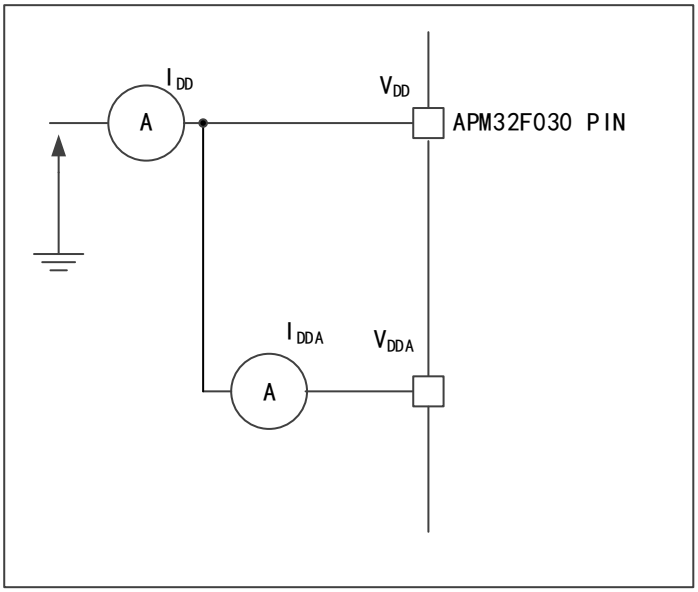


Figure 10 Current consumption measurement scheme



5.2. Absolute maximum rating

If the load on the device exceeds the absolute maximum rating, it may cause permanent damage to the device. Only the maximum load that can be borne is given here, and there is no guarantee that the device functions normally under this condition.

5.2.1 Maximum rated voltage characteristics

Table 21 **Maximum rated voltage characteristics**

Symbol	description	Minimum value	Maximum value	Unit
V_{DD}-V_{SS}	External main supply voltage (V_{DD}) (1)	-0.3	4.0	V
	External analog supply voltage (V_{DDA})	-0.3	4.0	
V_{DD}-V_{DDA}	Voltage difference allowed by V_{DD}>V_{DDA}	-	0.4	
V_{IN} (2)	Input voltage on FT and FTf pins (2)	V_{SS}-0.3	V_{DD}+4.0	
	Input voltage on TTa pin (2)	V_{SS}-0.3	4.0	
	BOOT0	0	V_{DD}+4.0	
	Input voltage on any other pin	V_{SS}-0.3	4.0	
$\|\Delta V_{DDx}\|$	Voltage difference between different power supply pins	-	50	mV
$\|V_{SSx}$-$V_{SS}\|$	Voltage difference between different grounding pins	-	50	

Note:

(1) All power supply (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the power supply within the external limited range.

(2) If V_{IN} is within the maximum range, $I_{INJ(PIN)}$ will not exceed its limit. If V_{IN} exceeds the maximum value, the value of $I_{INJ(PIN)}$ must be externally limited to ensure that its maximum value is not exceeded. The forward injection current appears when V_{IN} is greater than V_{DD}, while the reverse injection current appears when V_{IN} is less than V_{SS}.

5.2.2 Maximum Rated Current Features

Table 22 **Maximum Rated Current Features**

Symbol	Description	Maximum	Unit
ΣI_{VDD}	Total current into sum of all V_{DD} power lines (source)(1)	120	mA
ΣI_{VSS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	-120	
$I_{VDD(PIN)}$	Maximum current into each V_{DD} power pin (source) (1)	100	
$I_{VSS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	

	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	80	
	Total output current sourced by sum of all I/Os and control pins(2)	-80	
$I_{INJ(PIN)}$ (3)	Injected current on FT and FTf pins	-5/+0(4)	
	Injected current on TC and RST pins	±5	
	Injected current on TTa pins(5)	±5	
$\Sigma I_{INJ(PIN)}$(2)	Total injected current (sum of all I/O and control pins)(6)	±25	

Note:

(1) All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to a power supply within the external allowable range.

(2) If V_{IN} does not exceed the maximum value, $I_{INJ(PIN)}$ will not exceed its limit. If VIN exceeds the maximum value, $I_{INJ(PIN)}$ must be externally limited to not exceed its maximum value. When $V_{IN} > V_{DD}$, there is a forward injection current; when $V_{IN} < V_{SS}$, there is a reverse injection current.

(3) Reverse injection current can interfere with the analog performance of the ADC.

(4) When several I/O ports have injection current at the same Time, the maximum value of $\Sigma I_{INJ(PIN)}$ is the sum of the instantaneous absolute values of the forward injection current and the reverse injection current. These results are based on the calculation of the maximum value of $\Sigma I_{INJ(PIN)}$ on the four I/O port pins of the device.

(5) On these I/Os, a positive injection is induced by $V_{IN} > V_{DDA}$. Negative injection disturbs the analog performance of the device.

(6) When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

5.2.3 Maximum electrostatic characteristics

Table 23 **Electrostatic discharge (ESD)**

Symbol	Parameter	Condition	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (manikin)	T_A=+25°C	4500	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging equipment model)	T_A=+25°C	2000	

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.2.4 Static latch

Table 24 **Static latch**

Symbol	Parameter	Condition	Type
LU	Static latch class	T_A=+25°C/105°C	class ⅡA

5.2.5 Maximum temperature characteristics

Table 25 **Temperature characteristics**

Symbol	description	Numerical value	Unit
T_{STG}	Storage temperature range	–65~ +150	°C
T_J	Maximum junction temperature	150	°C

5.3. Testing under general working conditions

Table 26 **General working conditions**

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
F_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK}	Internal APB clock frequency	-	0	48	
V_{DD}	Standard operating voltage	-	2	3.6	V
V_{DDA}	Analog partial operating voltage	V_{DDA} must not be less than V_{DD}	2.4	3.6	V
V_{IN}	I/O input voltage	TC and RSTI/O	-0.3	V_{DD}+0.3	V
		TTa I/O	-0.3	V_{DDA}+0.3	
		FT and FTf I/O	-0.3	5.5	
		BOOT0	0	5.5	

5.3.1 Embedded reset and power control module characteristic test

The parameters given in Table 27 are derived from the test results under the

conditions of ambient temperature and power supply voltage summarized in Table 26.

Table 27 **Embedded reset and power control module features**

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
$V_{POR/PDR}$(1)	Power-on/power-down reset threshold	Falling edge (2)	-	1.87	-	V
		Rising edge	-	1.92	-	V
$V_{PDRhyst}$(3)	PDR hysteresis	-	-	50	-	mV
$T_{RSTTEMPO}$(3)	Reset duration	-	1.70	2.51	3.32	ms

Note:

(1) PDR detector monitors V_{DD} and V_{DDA} (if enabled in option byte), POR detector monitors V_{DD} only.

(2) Product characteristics are guaranteed by design to the minimum $V_{POR/PDR}$ value

(3) Guaranteed by design and not tested in production.

5.3.2 Built-in reference voltage characteristic test

The parameters given in Table 28 are derived from the test results under the conditions of ambient temperature and power supply voltage summarized in Table 26.

Table 28 **Built-in reference voltage**

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{REFINT}	Built-in reference voltage	-40°C < T_A < +105°C	1.19	1.20	1.23	V
t_{START}	ADC_IN17 buffer startup time	-	-	-	10	μs
$T_{S\_vrefint}$	Sampling time of ADC when reading out internal reference voltage	-	4	-	-	μs
ΔV_{REFINT}	Built-in reference voltage extends to temperature range	V_{DDA}=3.3V	-	-	10	mV

5.3.3 Power consumption

Power consumption test environment:

（1） Execute Dhrystone2.1, the compiling environment is KeilV5 and the compiling optimization level is L0.

(2) All I/O pins are configured as analog inputs and are connected to a static level of V_{DD} or V_{SS} (non-loaded).

(3) Unless otherwise specified, all peripherals are turned off.

(4) The relationship between Flash waiting period setting and f_{HCMU}: 0~24MHz—0 waiting period, 24~48MHz—1 waiting period.

(5) When it is greater than 24MHz, the instruction prefetch function is enabled (Note: this bit must be set before clock setting and bus frequency division).

(6) When the peripheral is turned on: $f_{PCLK}=f_{HCLK}$.

Table 29 **The program is executed in Flash, and the running mode consumes power**

Parameter	Condition	f_{HCMU}	Typical value (1)		Maximum value (1)	
			T_A=25°C, V_{DD}=3.3V		T_A=105°C, V_{DD}=3.6V	
			I_{DDA} (μA)	I_{DD}(mA)	I_{DDA}(μA)	I_{DD}(mA)
Running mode	External clock (2), enabling all peripherals	48MHz	105.69	10.0	125.76	10.39
		24MHz	59.64	5.67	74.78	5.88
		8MHz	1.44	2.31	7.7	2.43
	External clock (2), turn off all peripherals	48MHz	105.73	6.94	125.99	7.18
		24MHz	59.7	4.17	75.09	4.29
		8MHz	1.45	1.80	7.15	1.90
	Internal clock to enable all peripherals	48MHz	161.22	9.6	187.84	10.04
		24MHz	115.39	5.24	137.09	5.45
		8MHz	57.97	1.88	72.8	1.97
	Internal clock, turn off all peripherals	48MHz	161.54	6.51	187.58	6.82
		24MHz	115.50	3.66	136.98	3.85
		8MHz	58.0	1.33	72.45	1.40

Note:

(1) Data based on comprehensive evaluation will not be tested in production unless otherwise specified.

(2) The external clock is 8MHz. when f_{HCMU}>8MHz, PLL is started.

Table 30 **The program is executed in SRAM, and the running mode consumes power**

Parameter	Condition	f_{HCMU}	Typical value (1)		Maximum value (1)	
			T_A=25°C, V_{DD}=3.3V		T_A=105°C, V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA)	I_{DDA}(μA)	I_{DD}(mA)
Running mode	External clock (2), enabling all peripherals	48MHz	105.73	7.48	125.63	7.75
		24MHz	59.67	4.08	74.76	4.30

Parameter	Condition	f_{HCMU}	Typical value (1)		Maximum value (1)	
			T_A=25°C, V_{DD}=3.3V		T_A=105°C, V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA)	I_{DDA}(μA)	I_{DD}(mA)
		8MHz	1.44	1.8	7.20	1.88
	External clock (2), turn off all peripherals	48MHz	105.78	4.40	125.98	4.60
		24MHz	59.71	2.54	74.96	2.69
		8MHz	1.45	1.27	7.11	1.35
	Internal clock to enable all peripherals	48MHz	161.43	7.06	187.25	7.39
		24MHz	115.40	3.65	136.83	3.85
		8MHz	57.99	1.37	72.45	1.43
	Internal clock, turn off all peripherals	48MHz	161.62	3.94	187.61	4.14
		24MHz	115.49	2.07	137.02	2.23
		8MHz	58.04	0.79	72.4	0.86

Note:

(1) According to the comprehensive evaluation, it is not tested in production.

(2) The external clock is 8MHz. when f_{HCMU}>8MHz, PLL is started.

Table 31 **Program is executed in SRAM or Flash, power consumption in sleep mode**

Parameter	Condition	f_{HCMU}	Typical value (1)		Maximum value (1)	
			T_A=25°C, V_{DD}=3.3V		T_A=105°C, V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA)	I_{DDA}(μA)	I_{DD}(mA)
Sleep mode	External clock (2), enabling all peripherals	48MHz	105.77	5.41	125.88	5.54
		24MHz	59.70	3.03	74.91	3.16
		8MHz	1.45	1.42	7.12	1.50
	External clock (2), turn off all peripherals	48MHz	105.86	2.0	125.9	2.13
		24MHz	59.8	1.35	75.08	1.47
		8MHz	1.44	0.84	7.14	0.94
	Internal clock to enable all peripherals	48MHz	161.55	4.93	187.25	5.14
		24MHz	115.48	2.60	136.87	2.72
		8MHz	58.0	0.99	72.41	1.05
	Internal clock, turn off all peripherals	48MHz	161.71	1.52	187.85	1.69
		24MHz	115.54	0.86	137.13	0.99
		8MHz	58.0	0.37	72.35	0.46

Note:

(1) According to the comprehensive evaluation, it is not tested in production.

(2) The external clock is 8MHz. when f_{HCMU}>8MHz, PLL is started.

Table 32 **Power consumption in halt and standby mode**

Parameter	Condition		Typical value (T_A=25°C)				Maximum value (1) (T_A=105°C)	
			V_{DD}=2.4 V		V_{DD}= 3.3V		V_{DD}=3.6 V	
			I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)
halt mode	V_{DDA} monitoring ON	The voltage regulator is in running mode, and the low-speed and high-speed internal RC oscillators and high-speed oscillators are off	2.43	21.1	2.98	21.9	7.0	62.6
		The voltage regulator is in low power consumption mode, and the low-speed and high-speed internal RC oscillators and high-speed oscillators are off	2.43	6.47	2.98	7.42	7.0	44.9
Standby mode		Low-speed internal RC oscillator and independent watchdog are on	2.62	2.42	3.33	3.72	6.63	22.2
		The low-speed internal RC oscillator and the independent watchdog are off	2.28	1.96	2.83	3.08	6.11	21.5
halt mode	V_{DDA} monitoring OFF	The voltage regulator is in low power consumption mode, and the low-speed and high-speed internal RC oscillators and high-speed oscillators are off	1.25	6.33	1.45	7.38	5.13	44.9
Standby mode		Low-speed internal RC oscillator and independent watchdog are on	1.45	2.36	1.80	3.7	4.98	22.2
		The low-speed internal RC oscillator and the independent watchdog are off	1.10	1.93	1.31	3.05	4.44	21.5

Note: According to the comprehensive evaluation, it is not tested in production.

5.3.4 External clock source characteristics

High Speed External Clock Generated by Crystal Resonator (HSECLK osc)

For detailed parameters (frequency, package, precision, etc.) of crystal

resonator, please consult the corresponding manufacturer.

Table 33 **Characteristics of HSECLK 4~32MHz Oscillator (1)**

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistance	-	-	200	-	kΩ
I_{DD}	HSECLK current consumption	V_{DD} = 3.3 V, R_m = 45 Ω, C_L = 10 pF@8 MHz	-	660	-	μA
$t_{SU(HSECLK)}$	Startup time	V_{DD} is stable		1.7		ms

Note: It is guaranteed by design and has not been tested in production.

Low Speed External Clock (LSECLK osc) Generated by Crystal Resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 34 **LSECLK oscillator characteristics (f_{LSECLK}=32.768KHz) (1)**

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
I_{DD}	LSECLK current consumption	High driving ability		1.5		μA
$t_{SU(LSECLK)}$(2)	Startup time	V_{DDIOx} is stable	-	2	-	s

Note:

(1) Guaranteed by design and not tested in production.

(2) $t_{SU(HSECLK)}$ is the starting time, which is measured from the time when LSECLK is enabled by software to the time when stable oscillation at 32.768KHz is obtained. This value is measured using a standard crystal resonator, which may vary greatly due to different crystal manufacturers.

5.3.5 Internal clock source characteristics

Test of high speed internal (HSICLK)RC oscillator

Table 35 **HSICLK oscillator characteristics**

Symbol	Parameter	Condition		Minimum value	Typical value	Maximum value	Unit
f_{HSICLK}	Frequency	-		-	8	-	MHz
$A_{CCHSICLK}$	Accuracy of HSICLK oscillator	Factory calibration	V_{DD}=3.3V T_A=-25°C	-1	-	1	%
			V_{DD}=2-3.6V T_A=-40~105°C	-5	-	5	%

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
$t_{SU(HSICLK)}$	HSICLK oscillator start-up time	V_{DD}=3.3V T_A=-40~105°C	-	-	2	μs
$I_{DDA(HSICLK)}$	HSICLK oscillator power consumption	-	-	60	-	μA

Note: According to the comprehensive evaluation, it is not tested in production.

Table 36 **Characteristics of HSICLK14 oscillator**

Symbol	Parameter	Condition		Minimum value	Typical value	Maximum value	Unit
$f_{HSICLK14}$	Frequency	-		-	14	-	MHz
$Acc_{HSICLK14}$	Accuracy of HSICLK14 oscillator	Factory calibration	V_{DD}=3.3V T_A=-25°C	-1	-	1	%
			V_{DD}=2-3.6V T_A=-40~105°C	-5	-	5	%
$t_{SU(HSICLK14)}$	Starting time of HSICLK14 oscillator	V_{DD}=3.3V T_A=-40~105°C		-	-	2	μs
$I_{DDA(HSICLK14)}$	Power consumption of HSICLK14 oscillator	-		-	72	-	μA

Note: According to the comprehensive evaluation, it is not tested in production.

Low speed internal (LSICLK)RC oscillator test

Table 37 **LSICLK oscillator characteristics**

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
f_{LSICLK}	Frequency (V_{DD} =2-3.6V, T_A =-40 ~ 105 C)	30	40	50	KHz
$t_{SU(LSICLK)}$	Startup time of LSICLK oscillator (V_{DD}=3.3V, T_A=-40~105°C)	-	30	-	μs
$I_{DD(LSICLK)}$	LSICLK oscillator power consumption	-	0.5	-	μA

Note: According to the comprehensive evaluation, it is not tested in production.

5.3.6 Wake-up time in low power mode

Table 38 **Awakening clock source parameters**

Symbol	Parameter	Typical value	Unit
$t_{WUSLEEP}$	Wake up from sleep mode	4 SYSCLK cycles	μs
t_{WUSTOP}	Wake up from halt mode	3.1	
$t_{WUSTDBY}$	Wake up from standby mode	40	

Note: The wake-up time is measured from the start of the wake-up event to the first instruction read by the user program.

5.3.7 PLL characteristics

Table 39 **PLL characteristics**

Symbol	Parameter	Numerical value (1)			Unit
		Minimum value	Typical value	Maximum value	
f_{PLL_IN}	PLL input clock	1	8	24	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL frequency doubling output clock (V_{DD}=3.3V，T_A=-40~105°C)	16	-	48	MHz
t_{LOCK}	PLL phase locking time	-	-	90	μs

Note: According to the comprehensive evaluation, it is not tested in production.

5.3.8 Memory characteristics

flash memory

Table 40 **FLASH memory characteristics**

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{prog}	16-bit programming time	T_A =-40~105°C V_{DD}=2.0~3.6V	-	17.9	-	μs
t_{ERASE}	Page (1Kbytes) erase time	T_A=-40~105°C V_{DD}=2.0~3.6V	-	1.56	-	ms
t_{ME}	Whole erase time	T_A=25°C V_{DD}=3.3V	-	6.4	-	ms
V_{prog}	Programming voltage	T_A=-40~105°C	2.0	3.3	3.6	V
t_{RET}	Data saving time	T_A=55℃	20	-	-	years
N_{RW}	Erase cycle	T_A=25°C	10K	-	-	cycles

Note: According to the comprehensive evaluation, it is not tested in production.

5.3.9 I/O port characteristics

Table 41 **Dc characteristics (T_A =-40℃-105℃, V_{DD} = 2 ~ 3.6 v)**

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{IL}		TC and TTa I/O	-	-	0.3V_{DD}+0.1	V
		FT and FTf I/O	-	-	0.476V_{DD}-0.4	

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
	Input low level voltage	I/O pins except BOOT0 pin	-	-	$0.3V_{DD}$	
V_{IH}	Input high level voltage	TC and TTa I/O	$0.447V_{DD}+0.402$	-	-	V
		FT and FTf I/O	$0.5V_{DD}+0.2$	-	-	
		I/O pins except BOOT0 pin	$0.7V_{DD}$	-	-	
V_{hys}	Schmidt trigger hysteresis	TC and TTa I/O		200		mV
		FT and FTf I/O		300		
I_{lkg}	Input leakage current	TC, FT and FTf I/O TTa in digital mode $V_{SS}\leq V_{IN}\leq V_{DDIOx}$	-	-	±0.1	μA
		TTa in digital mode $V_{DDIOx}\leq V_{IN}\leq V_{DDA}$	-	-	1	
		TTa in analog mode $V_{SS}\leq V_{IN}\leq V_{DDA}$	-	-	±0.1	
		FT and FTf I/O (1) $V_{DDIOx}\leq V_{IN}\leq 5V$	-	-	10	
R_{PU}	Weak pull-up equivalent resistance	$V_{IN}=V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistance	$V_{IN}=V_{DDIOx}$	30	40	50	kΩ

Table 42 **Ac characteristics (T_A = 25 c)**

MODEx[1:0] Configuration of	Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
10 (2MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=50 pF, V_{DD}=2.4~3.6V	-	2	MHz
	$t_{f(IO)out}$	Output high to low fall time	C_L=50 pF, V_{DD}=2.4~3.6V	-	125	ns
	$t_{r\ (IO)out}$	Output rise time from low to high level		-	125	

MODEx[1:0] Configuration of	Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
01 (10MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=50 pF, V_{DD}=2.4~3.6V	-	10	MHz
	$t_{f(IO)out}$	Output high to low fall time	C_L=50 pF, V_{DD}=2.4~3.6V	-	25	ns
	$t_{r\ (IO)out}$	Output rise time from low to high level		-	25	
11 (50MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=30 pF, V_{DD}=2.7~3.6V	-	50	MHz
	$t_{f(IO)out}$	Output high to low fall time	C_L=30 pF, V_{DD}=2.7~3.6V	-	5	ns
	$t_{r\ (IO)out}$	Output rise time from low to high level		-	5	
FM+ configuration	$f_{max(IO)out}$	Maximum frequency (3)	C_L=50pF, V_{DDIOx} =2.4~3.6V	-	2	MHz
	$t_{f(IO)out}$	Output falling time		-	34	ns
	$t_{r(IO)out}$	Output rise time		-	34	

Figure 11 Definition of input and output AC characteristics

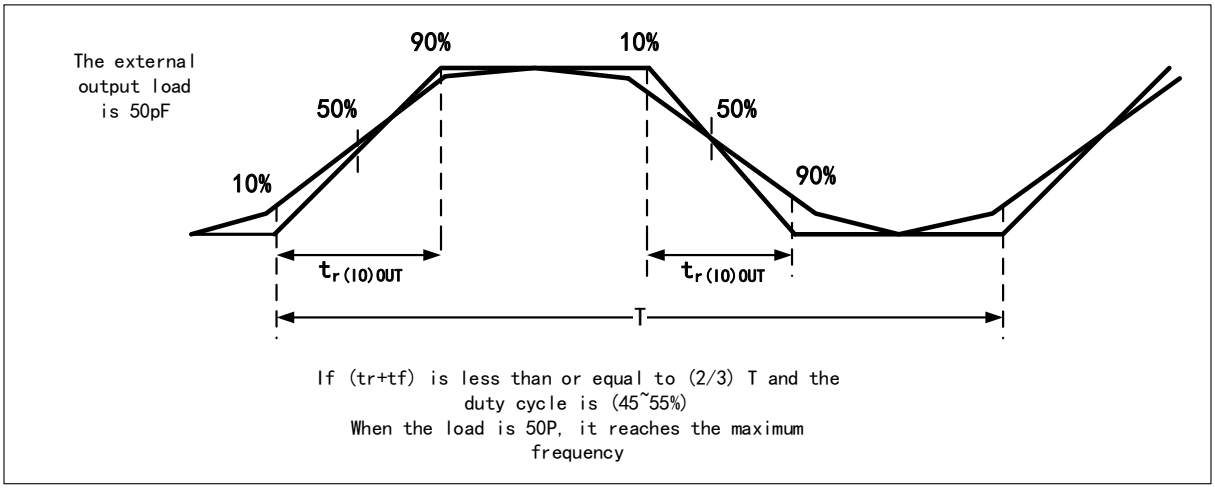


Table 43 **Output drive current characteristics (T_A=25°C)**

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
V_{OL}	I/O pin outputs low voltage	$\|I_{IO}\|$=8 mA V_{DDIOx}≥2.7V	-	0.4	V
V_{OH}	I/O pin outputs high voltage		V_{DDIOx}-0.4	-	
V_{OL}	I/O pin outputs low voltage	$\|I_{IO}\|$=20 mA V_{DDIOx}≥2.7V	-	1.3	V
V_{OH}	I/O pin outputs high voltage		V_{DDIOx}-1.3	-	

5.3.10 NRST pin characteristics

The NRST pin input drive adopts CMOS process, which is connected with a permanent pull-up resistor R_{PU}.

Table 44 **NRST pin characteristics (T_A =-40 ~ 105 C, V_{CC} = 2 ~ 3.6 V)**

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
$V_{IL(NRST)}$	NRST input low voltage	-	-	-	$0.31V_{DD}$+0.065	V
$V_{IH(NRST)}$	NRST input high voltage	-	$0.446V_{DD}$+0.405			
$V_{hys(NRST)}$	Voltage hysteresis of NRST Schmitt trigger	-	-	300	-	mV
R_{PU}	Weak pull-up equivalent resistance	V_{IN}=V_{SS}	30	40	50	kΩ

5.3.11 communication interface

I2C interface characteristics

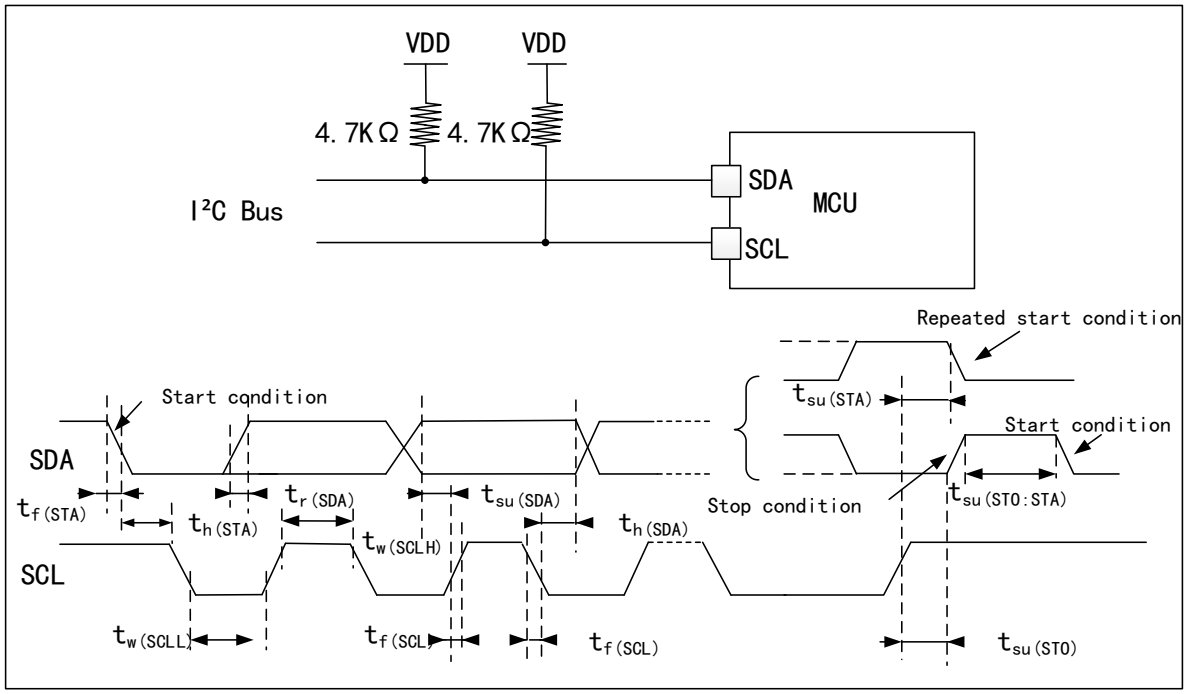
- Standard mode (Sm): bit rate up to 100kbit/s
- Fast mode (Fm): bit rate up to 400 kbit/s
- Ultra fast mode (Fm+): bit rate up to 1Mbit/s

Table 45 **I2C interface characteristics (T_A = 25°C, V_{DD} = 3.3 V)**

Symbol	Parameter	Standard I2C		Fast I2C		Ultrafast I2C		Unit
		Minimum value	Maximum value	Minimum value	Maximum value	Minimum value	Maximum value	
$t_{w(SCLL)}$	SCL clock low time	4.84	-	1.21	-	0.52	-	μs
$t_{w(SCLH)}$	SCL clock high time	5.09	-	1.14	-	0.46	-	
$t_{su(SDA)}$	SDA setup time	4460	-	860	-	321	-	ns
$t_{h(SDA)}$	SDA data holding time	103	181	0	252	0	145	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	500	-	300	-	120	
$t_{f(SDA)}$ /$t_{f(SCL)}$	SDA and SCL fall time	-	9.86	-	8.12	-	4	

Symbol	Parameter	Standard I2C		Fast I2C		Ultrafast I2C		Unit
		Minimum value	Maximum value	Minimum value	Maximum value	Minimum value	Maximum value	
$t_{h(STA)}$	Start condition holding time	4.96	-	1		0.33	-	μs
$t_{su(STA)}$	Repeated start condition setup time	5.16	-	1.21	-	0.64	-	
$t_{su(STO)}$	Setup time of stop condition	4.50	-	1.21	-	0.54	-	μs
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle)	4.67	-	1.37	-	0.77	-	μs

Figure 12 Bus AC waveform and measurement circuit



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

SPI interface characteristics

Table 46 **SPI characteristics (T_A = 25°C, V_{DD} = 3.3 V)**

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	holotype	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C = 15pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	223		ns
$t_{h(NSS)}$	NSS holding time	Slave mode	65		ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Main mode, f_{PCMU} = 36MHz, Prescaler coefficient =4	54	57	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	holotype	12		ns
		Slave mode	20		
$t_{h(MI)}$ $t_{h(SI)}$	Data input holding time	holotype	34		ns
		Slave mode	22		
$t_{a(SO)}$	Data output access time	In slave mode, f_{PCLK} = 20MHz		17	ns
$t_{dis(SO)}$	Data output prohibition time	Slave mode		18	ns
$t_{v(SO)}$	Effective time of data output	Slave mode (after enable edge)		16	ns
$t_{v(MO)}$	Effective time of data output	Master mode (after enable edge)		6	ns
$t_{h(SO)}$	Data output holding time	Slave mode (after enable edge)	11.5		ns
$t_{h(MO)}$		Master mode (after enable edge)	2		

Figure 13 SPI timing diagram—slave mode and CPHA=0

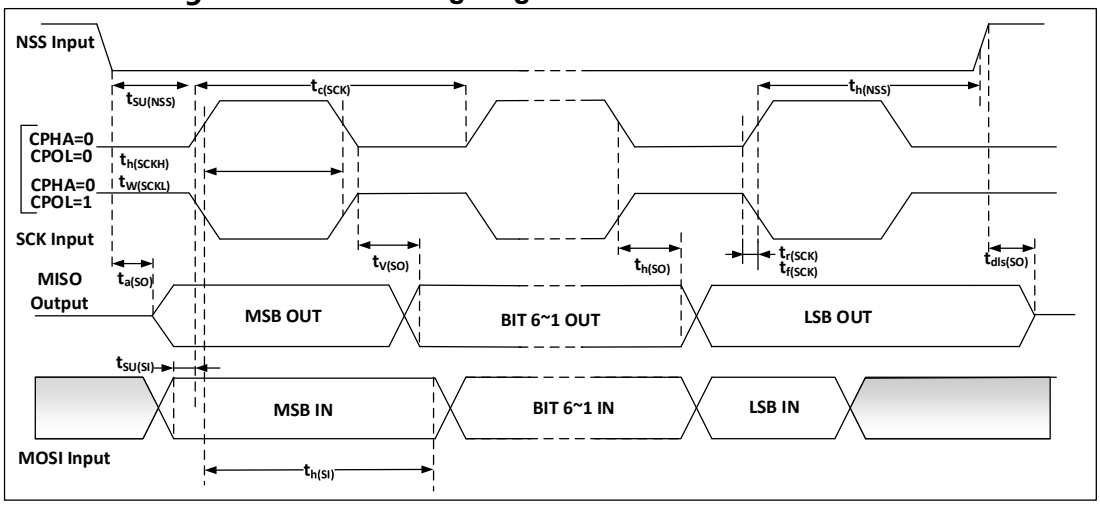
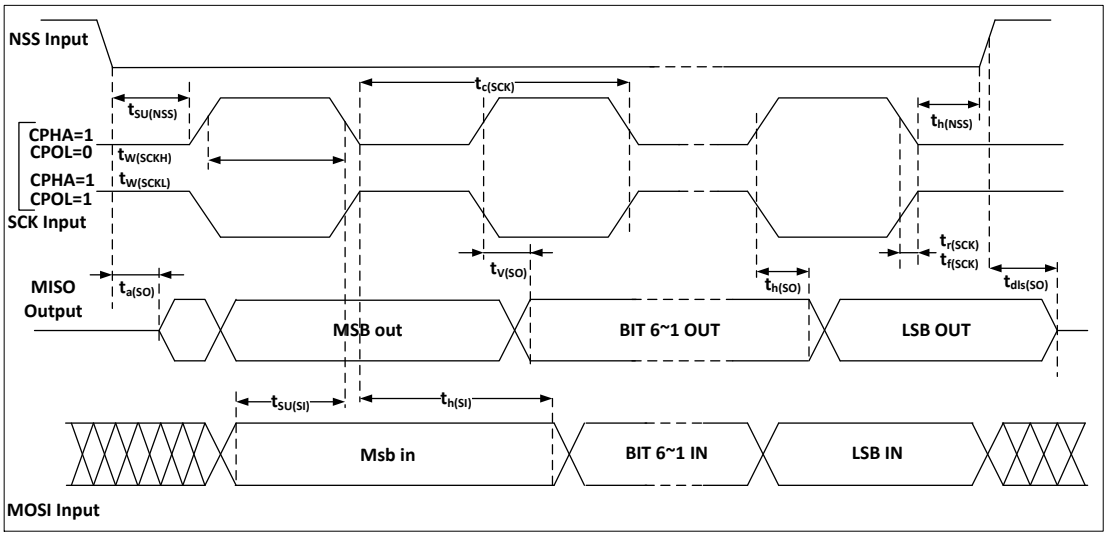
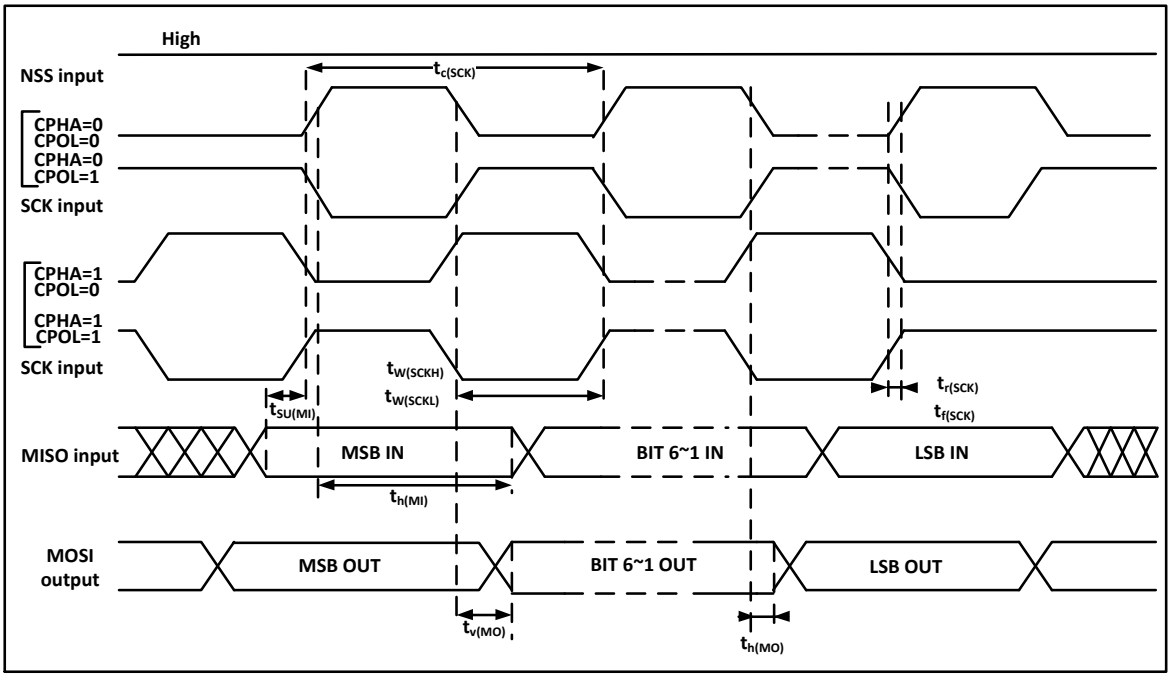


Figure 14 SPI timing diagram—slave mode and CPHA=1



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 15 SPI timing diagram—main mode



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.3.12 12-bit ADC features

Table 47 **12-bit ADC features**

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{DDA}	Service voltage	-	2.4	-	3.6	V
f_{ADC}	ADC frequency	-	0.6	-	14	MHz
C_{ADC}	Internal sampling	-	-	8	-	pF

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
	and holding capacitance					
R_{ADC}	Sampling resistance	-	-	-	1000	Ω
t_S	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	μs
T_{CONV}	Sampling and conversion Time	f_{ADC} = 14 MHz, 12-bit conversion	1	-	18	μs

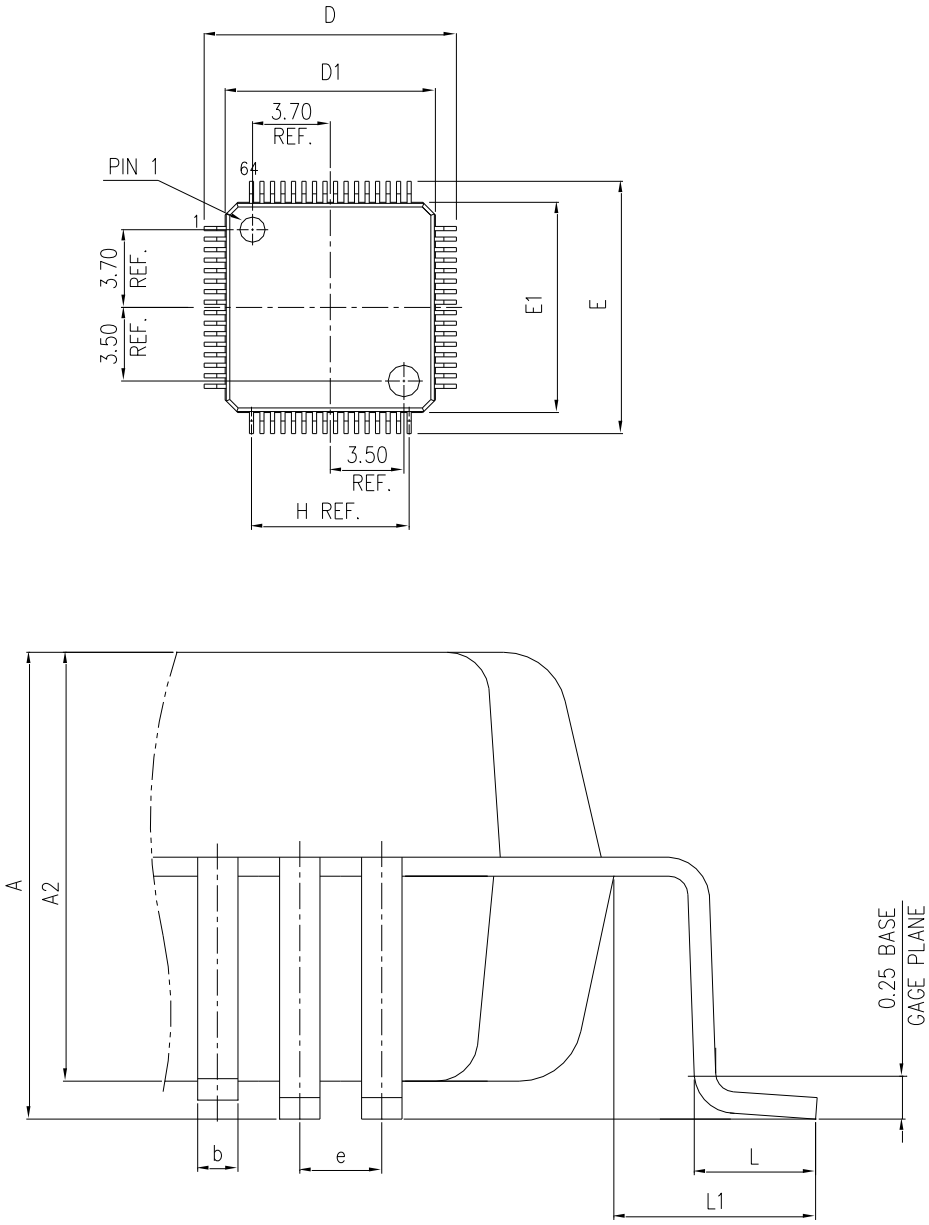
Table 48 **12-bit ADC accuracy**

Symbol	Parameter	Condition	Typical value	Maximum value	Unit
$\|E_T\|$	Composite error	f_{PCLK}=48M, f_{ADC}=14M, V_{DDA}=2.4V-3.6V T_A=-40℃~105℃	3.4	4.0	LSB
$\|E_O\|$	offset error		2.1	3	
$\|E_G\|$	Gain error		0.6	1.3	
$\|E_D\|$	Differential linear error		0.65	1.3	
$\|E_L\|$	Integral linearity error		1.32	1.65	

6. Package Characteristics

6.1. LQFP64 package information

Figure 16 LQFP64 package outline



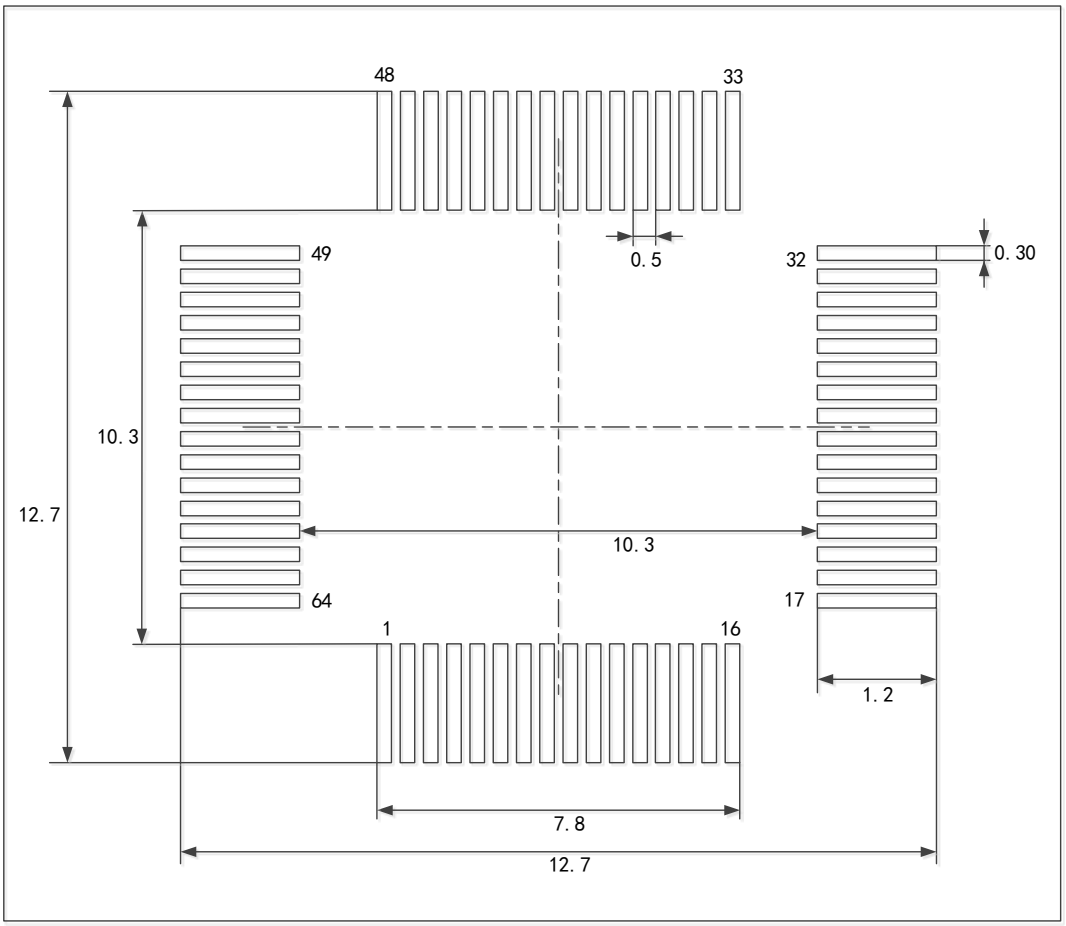
Note: The Figure is not drawn to scale.

Table 49 **Package dimensions of LQFP64**

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX.1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	12.000±0.200	LEAD TIP TO TIP
4	D1	10.000±0.100	PKG LENGTH
5	E	12.000±0.200	LEAD TIP TO TIP
6	E1	10.000±0.100	PKG WIDTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF.	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H(REF.)	(7.500)	GUM.LEAD PITCH
11	b	0.220±0.050	LEAD WIDTH

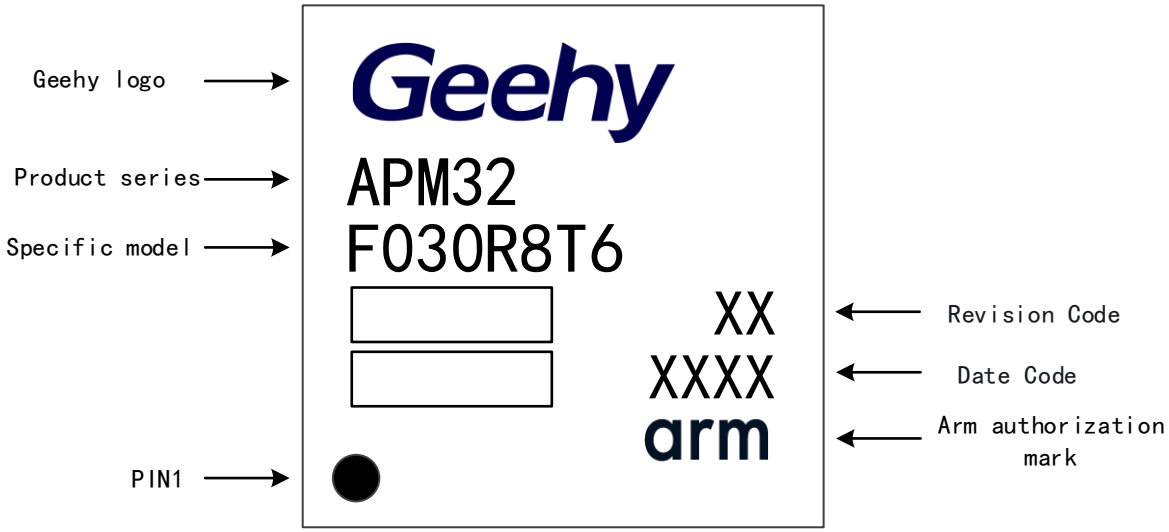
Note: The value in inches is converted from mm to 4 decimal places.

Figure 17 LQFP64 welding Layout suggestion



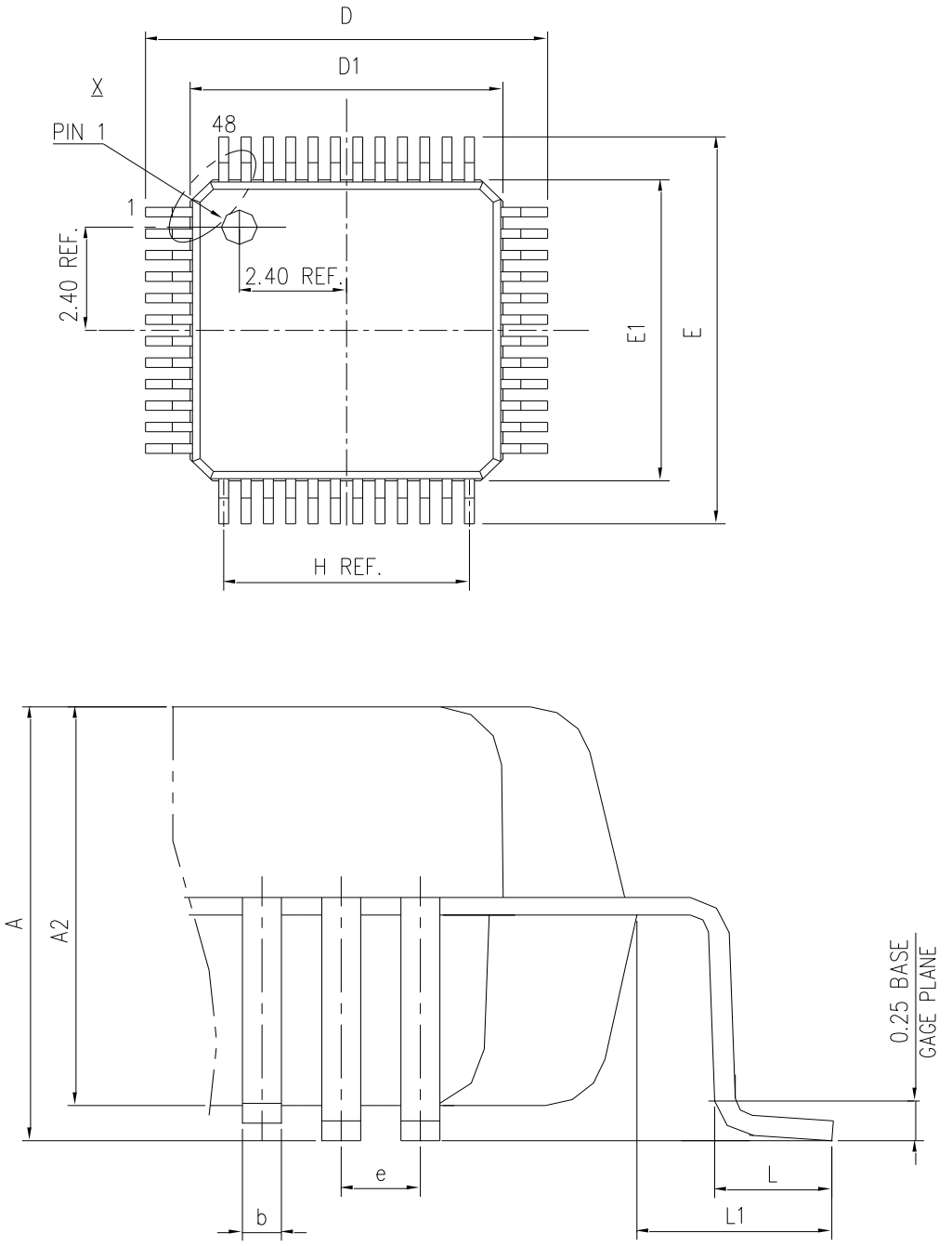
Note: Dimensions are in millimeters.

Figure 18 LQFP64 coding specification



6.2. LQFP48 package information

Figure 19 LQFP48 package outline



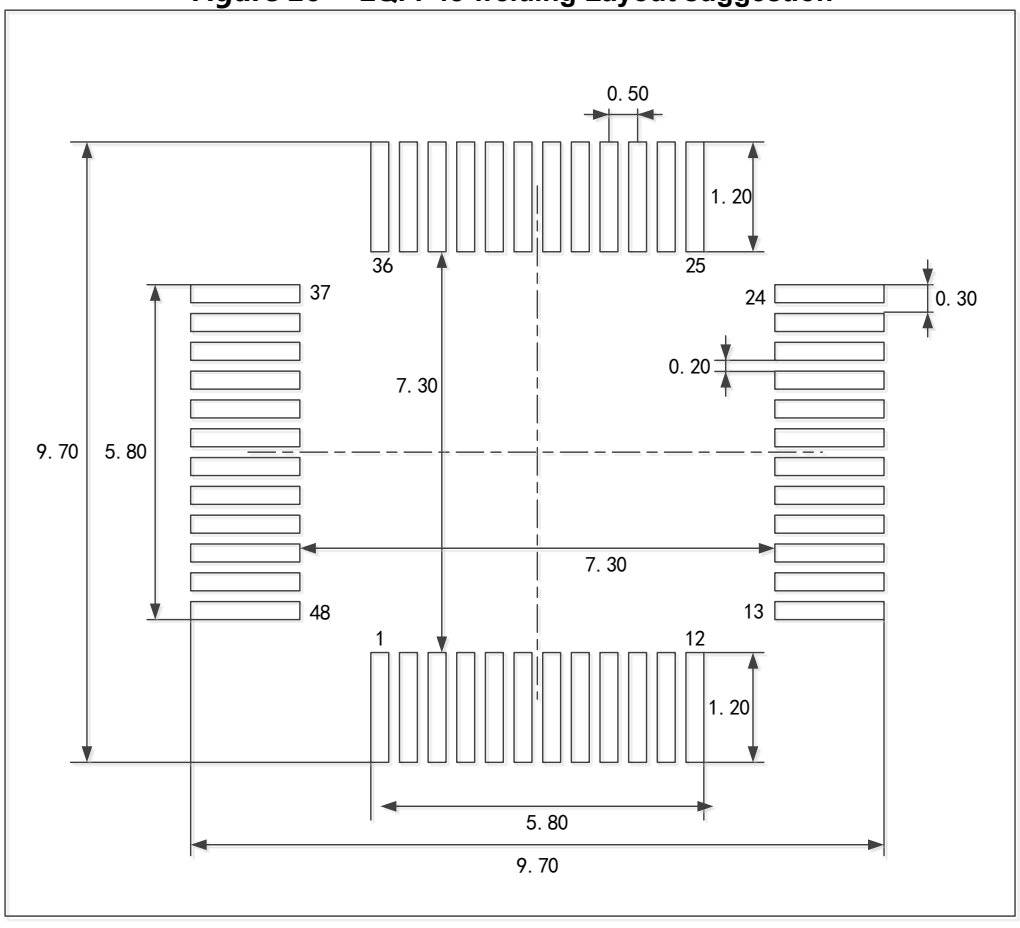
Note: The Figure is not drawn to scale.

Table 50 **Package dimensions of LQFP48**

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX.1.60	OVERALL HEIGHT
2	A2	1.40±0.05	PKG THICKNESS
3	D	9.00±0.20	LEAD TIP TO TIP
4	D1	7.00±0.10	PKG LENGTH
5	E	9.00±0.20	LEAD TIP TO TIP
6	E1	7.00±0.10	PKG WIDTH
7	L	0.60±0.15	FOOT LENGTH
8	L1	1.00 REF.	LEAD LENGTH
9	e	0.50 BASE	LEAD PITCH
10	H(REF.)	(5.50)	GUM.LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

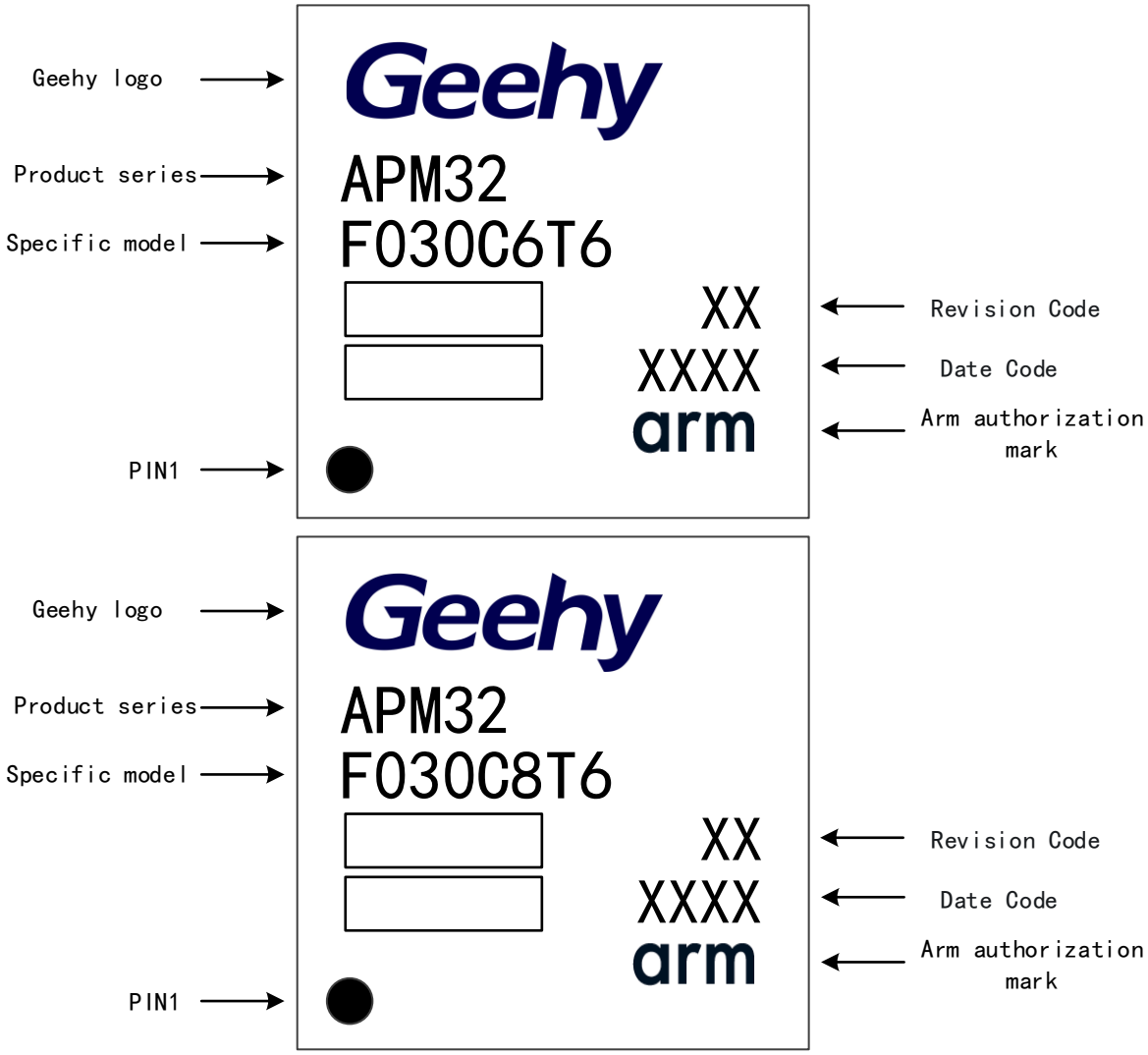
Note: The value in inches is converted from mm to 4 decimal places.

Figure 20 LQFP48 welding Layout suggestion



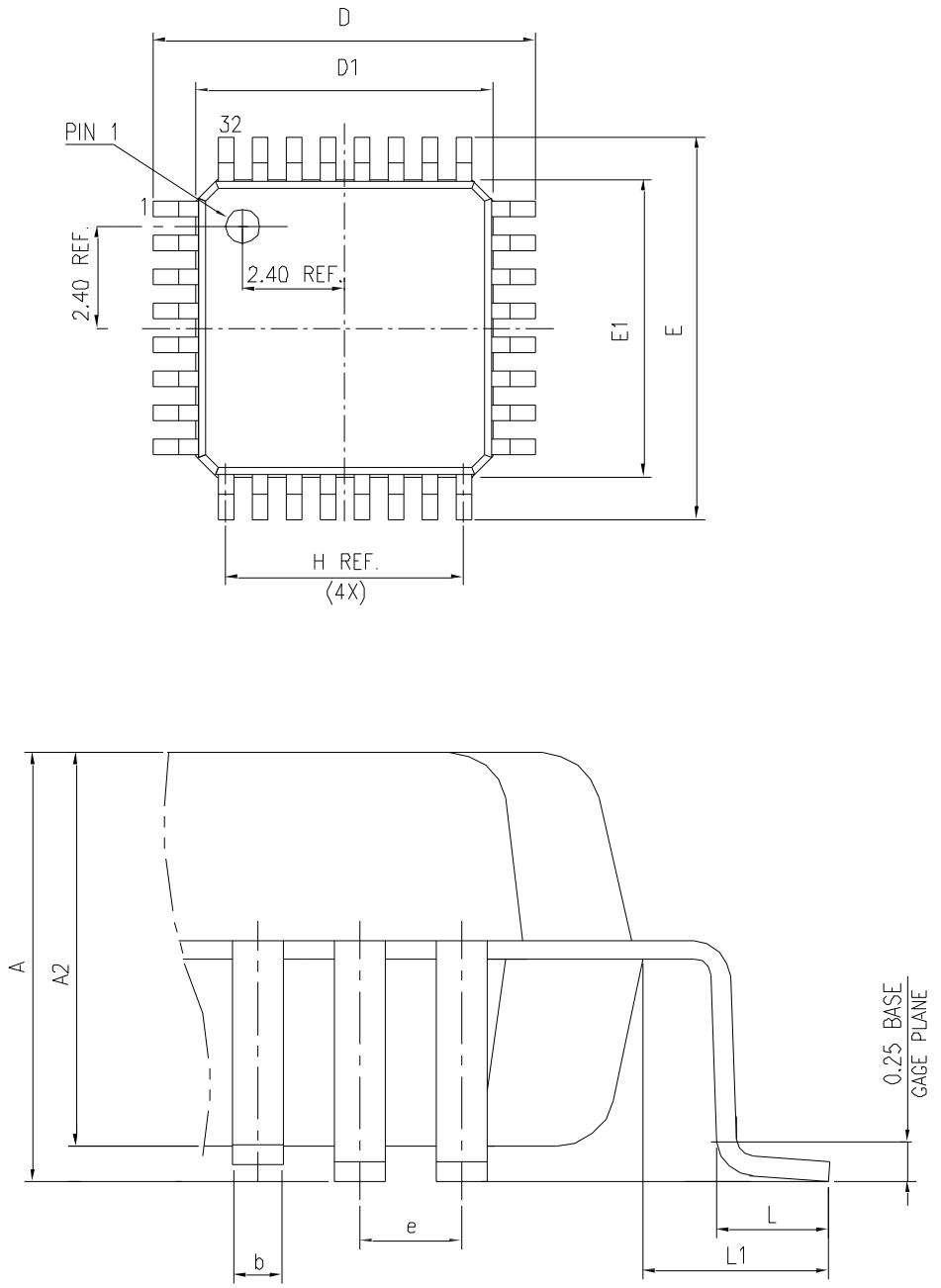
Note: Dimensions are in millimeters.

Figure 21 LQFP48 coding specification



6.3. LQFP32 package information

Figure 22 LQFP32 package outline



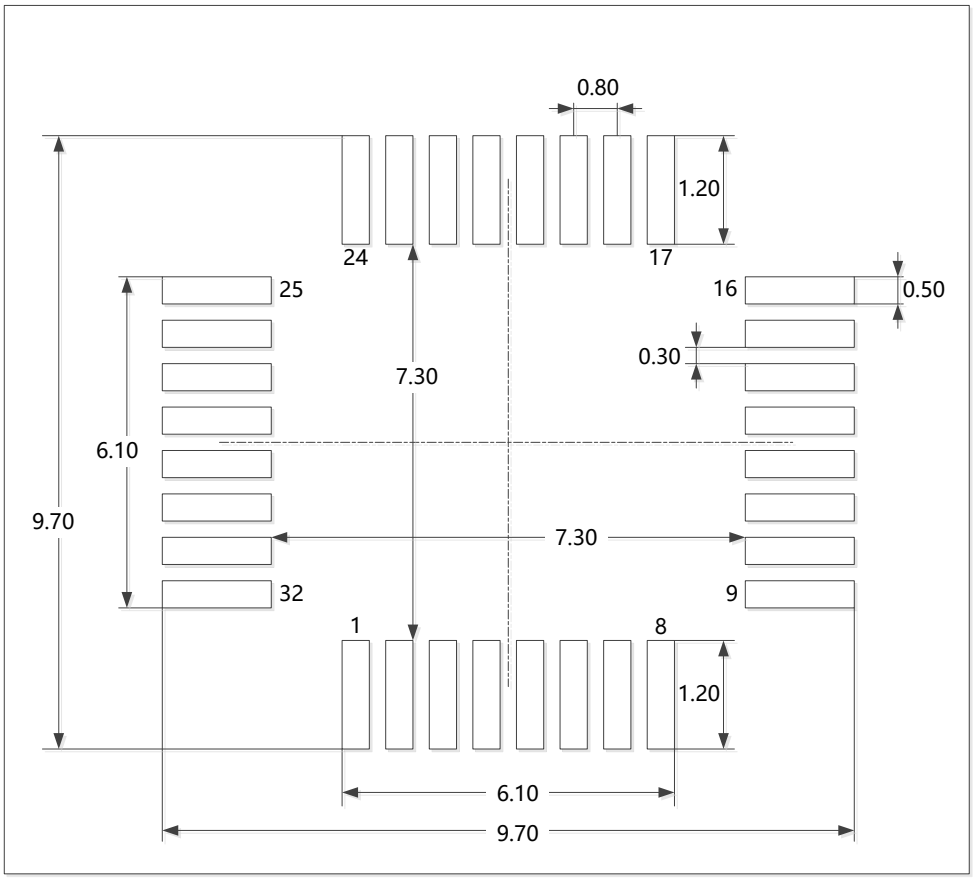
Note: The Figure is not drawn to scale.

Table 51 **Package dimensions of LQFP32**

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX.1.6	OVERALL HEIGHT
2	A2	1.40±0.05	PKG THICKNESS
3	D	9.00±0.20	LEAD TIP TO TIP
4	D1	7.00±0.10	PKG LENGTH
5	E	9.00±0.20	LEAD TIP TO TIP
6	E1	7.00±0.10	PKG WIDTH
7	L	0.60±0.15	FOOT LENGTH
8	L1	1.00 REF.	LEAD LENGTH
9	e	0.80 BASE	LEAD PITCH
10	H(REF.)	(5.60)	GUM.LEAD PITCH
11	b	0.370±0.080/0.070	LEAD WIDTH

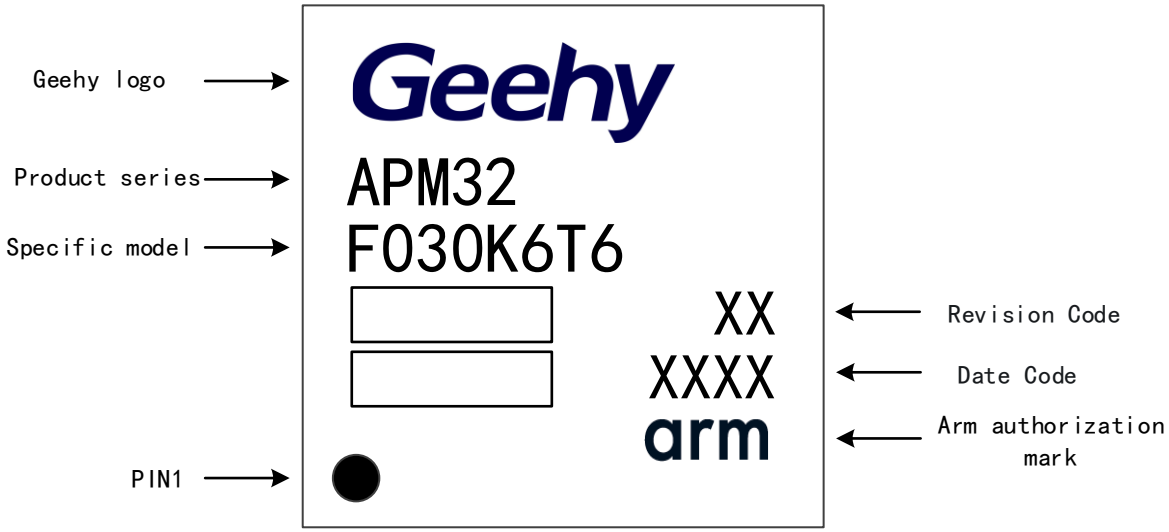
Note: The value in inches is converted from mm to 4 decimal places.

Figure 23 LQFP32 welding Layout suggestion



Note: Dimensions are in millimeters.

Figure 24 LQFP32 coding specification



6.4. QFN32 Package information

Figure 25 QFN32 package outline

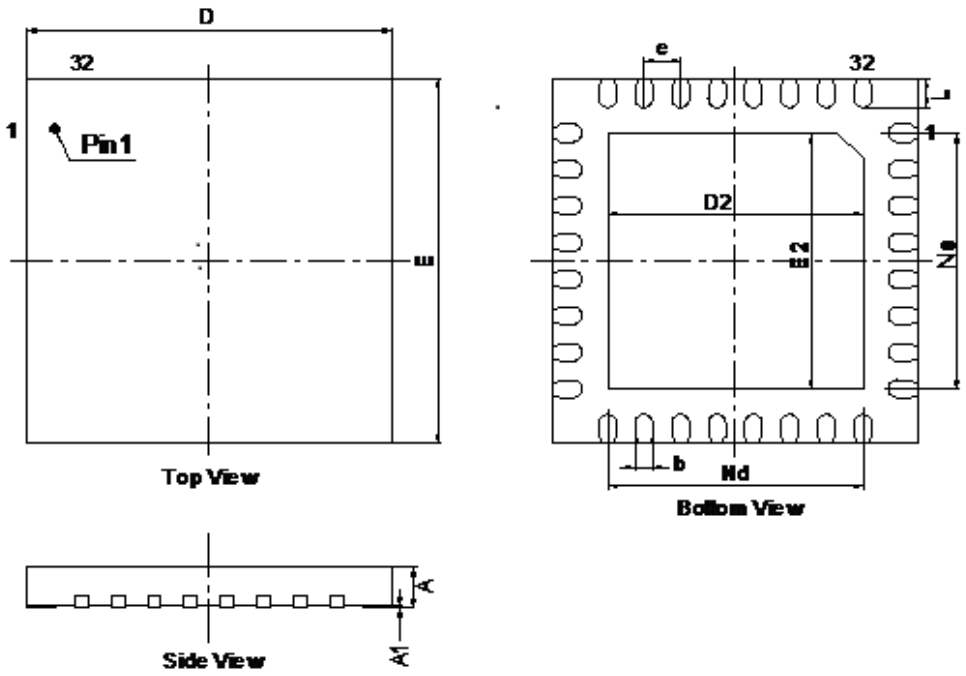


Table 52 QFN32 Package dimensions

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.5	0.55	0.6
A1	0	0.02	0.05

SYMBOL	MILLIMETER		
b	0.19	0.24	0.29
D	4.9	5	5.1
D2	3.4	3.5	3.6
e	0.50BSC		
Nd	3.50BSC		
E	4.9	5	5.1
E2	3.4	3.5	3.6
Ne	3.50BSC		
L	0.35	0.4	0.45

Figure 26 QFN32 welding Layout suggestion

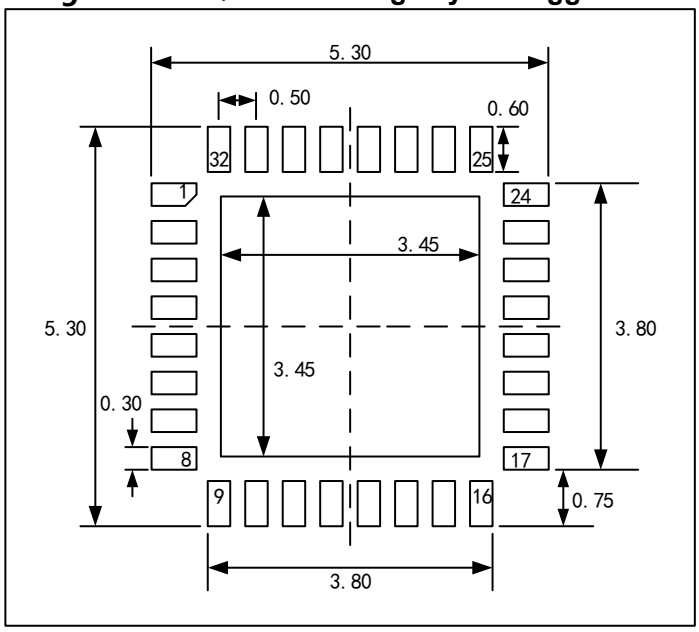
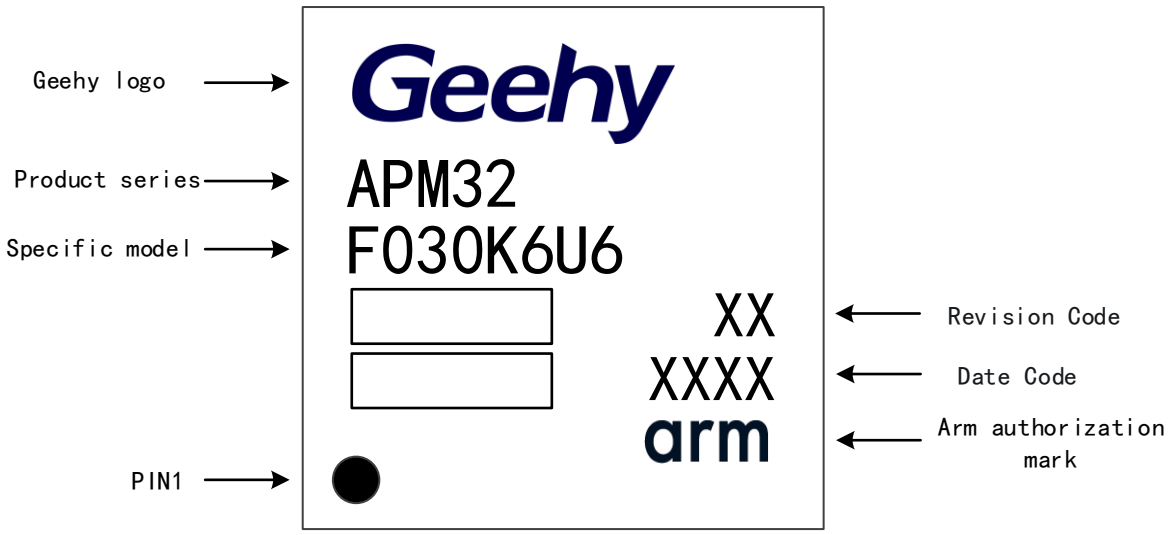


Figure 27 QFN32 Code specification



7. Ordering information

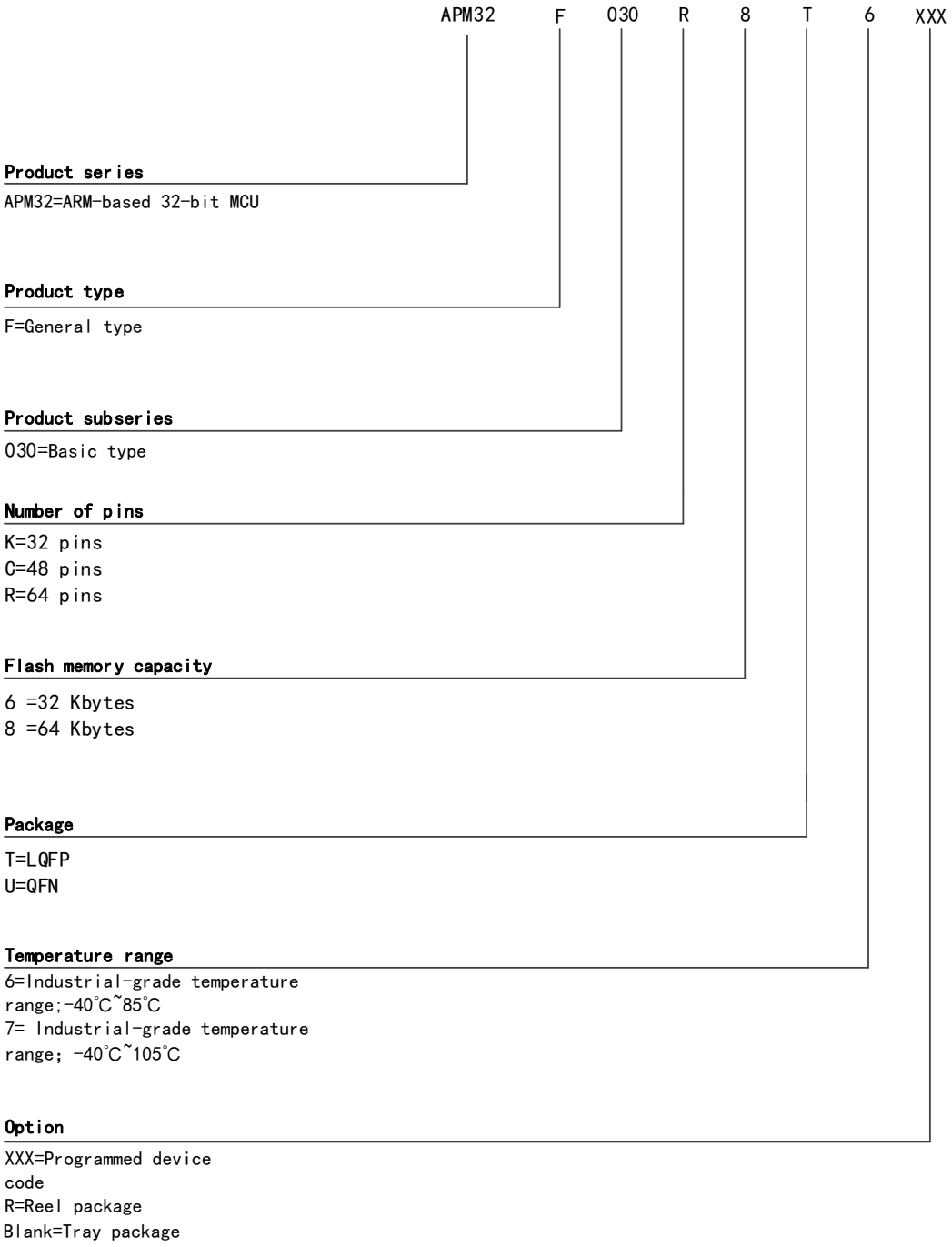


Table 53 **Order information list**

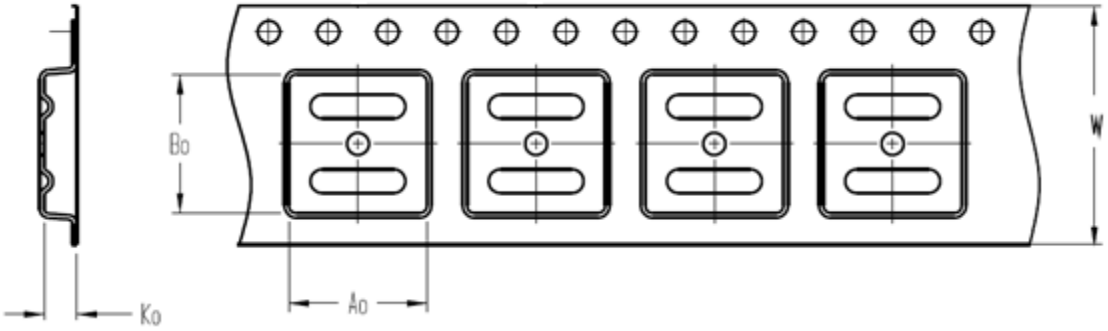
Order code	FLASH(KB)	SRAM(KB)	Package	SPQ	Temperature range
APM32F030K6U6-R	32	4	QFN32	5000	Industrial grade -40℃~85℃
APM32F030K6U6	32	4	QFN32	4900	Industrial grade -40℃~85℃
APM32F030K6T6-R	32	4	LQFP32	2000	Industrial grade -40℃~85℃
APM32F030K6T6	32	4	LQFP32	2500	Industrial grade -40℃~85℃
APM32F030K8T6-R	64	8	LQFP32	2000	Industrial grade -40℃~85℃
APM32F030K8T6	64	8	LQFP32	2500	Industrial grade -40℃~85℃
APM32F030C6T6-R	32	4	LQFP48	2000	Industrial grade -40℃~85℃
APM32F030C6T6	32	4	LQFP48	2500	Industrial grade -40℃~85℃
APM32F030C8T6-R	64	8	LQFP48	2000	Industrial grade -40℃~85℃
APM32F030C8T6	64	8	LQFP48	2500	Industrial grade -40℃~85℃
APM32F030R8T6-R	64	8	LQFP64	1000	Industrial grade -40℃~85℃
APM32F030R8T6	64	8	LQFP64	1600	Industrial grade -40℃~85℃

Note :SPQ= Minimum number of packages

8. Packaging information

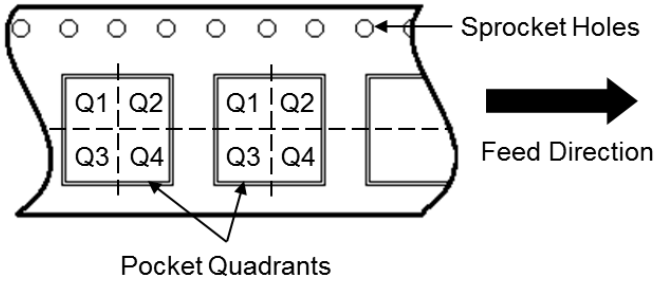
8.1. Reel packaging

Figure 28 Reel dimensions



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape

Quadrant Assignments for PIN1 Orientation in Tape



Reel Dimensions

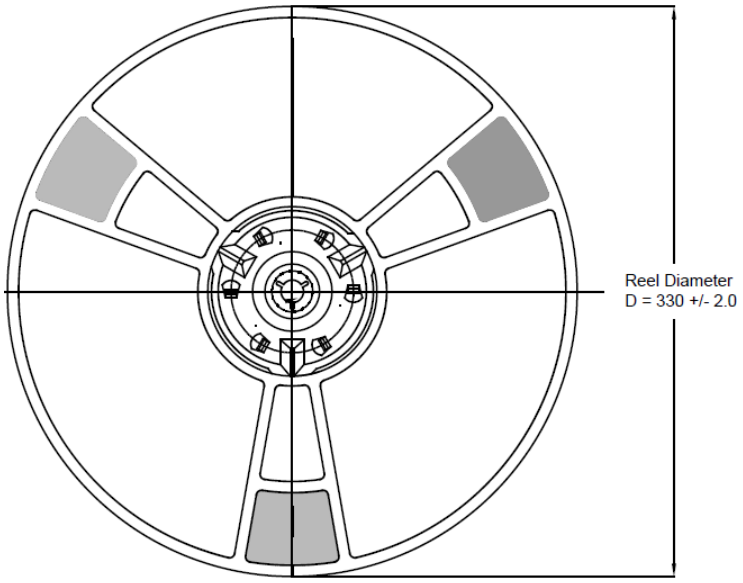
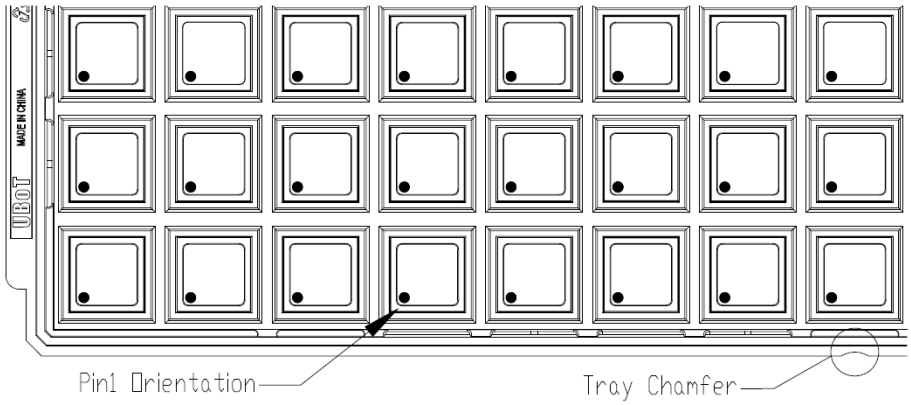


Table 54 **Reel packaging parameter specification table**

Package Type	Pins	SPQ	Reel Diameter (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
LQFP	48	2000	330	9.3	9.3	2.2	16	Q1
LQFP	32	2000	330	9.3	9.3	2.2	16	Q1
QFN	32	5000	330	5.3	5.3	0.8	12	Q1

8.2. Tray packaging

Figure 29 Tray packaging diagram



Tray Dimensions

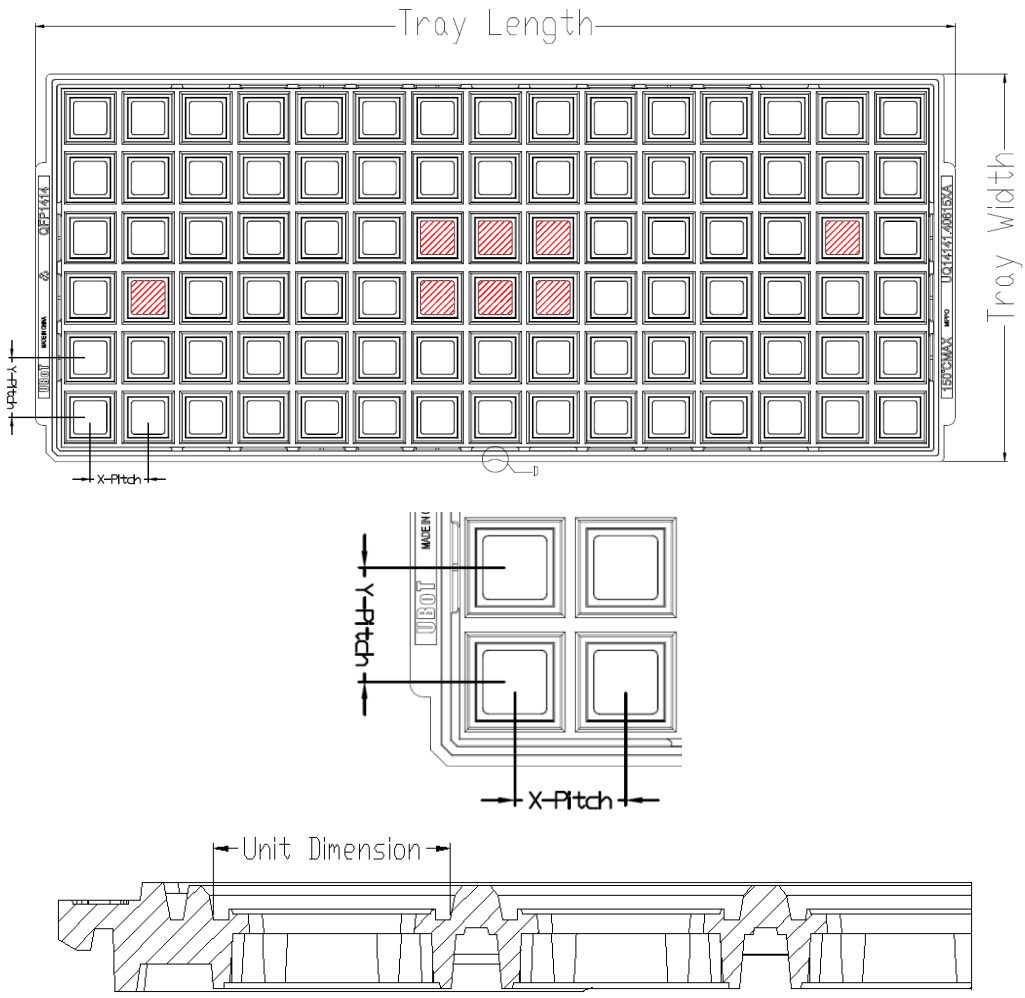


Table 55 **Tray packaging parameter specification table**

Device	Package Type	Pins	SPQ	X-Dimension (mm)	Y-Dimension (mm)	X-Pitch (mm)	Y-Pitch (mm)	Tray Length (mm)	Tray Width (mm)
APM32F030R8T6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F030C6T6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F030C8T6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F030K6T6	LQFP	32	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F030K8T6	LQFP	32	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F030K6U6	QFN	32	4900	5.2	5.2	8.7	9.0	322.6	135.9

9. Naming of common functional modules

Table 56 **Naming of common functional modules**

Naming of common functional modules	
Description in Chinese	**Abbreviations**
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management unit	RCM
External interrupt	EINT
Universal IO	GPIO
Multiplex IO	AFIO
Wake up controller	WUPT
Buzzer	BUZZER
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC controller	CRC
Power management unit	PMU
DMA controller	DMA
Digital analogue converter	ADC
Real-time clock	RTC
External memory controller	EMMC
Controller area network	CAN
I2C interface	I2C
serial peripheral interface	SPI
Universal asynchronous transceiver	UART
Universal asynchronous synchronous transceiver	USART
Flash interface control unit	FMC

10. Revision history

Table 58 **Document revision history**

Date	Revision	Change
2020.07.1	V1.0.0	New folder
2020.07.06	V1.0.1	Modify the cover page and directory format
2020.9.9	V1.1	(1) Modify the font (2) Modify the naming rules of Order Information *(Chapter 7), modify the order code in the order Information list table and add a column of the minimum number of packages (3) Modify the error in the Functional Description of APM32F030x6/x8 Pin table (4) Modify the Figure 27 Code Specification in the package information (Chapter 6)
2021.6.4	V1.2	(1) Modify HXT-HSECLK LXT-LSECLK HIRC-HSICLK LIRC-LSICLK (2) modified LSECLK osc for crystal resonator to produce low speed. (3) Modify the title of the recommended Layout diagram corresponding to QFN32. (4) Delete the temperature sensor module
2021.6.30	V1.3	Increase the maximum rated current characteristic