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TITLE ：NV173FHM-N4F

Customer: DELL

Product Specification

Rev. 0

(DELL DPN： 0VC9P0)

BOE Optoelectronics Technology Co., Ltd

REVISION HISTORY

( )Preliminary Specification

(√)Final Specification

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P2	31/36~39	Updated Label and EDID X10→X20	2020.01.06	Liu Xinghong
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REVIEWED	
Designer	**Manager**
Zhang Shouqiang(Array)	Wang Wu
Teng Zhenyuan(Cell)	Li Zhe
Zha Changjun(CF)	Li Min
Chen Yao(EE)	Xu Bo
Ge Shikang(MO)	Li Yucheng
Long Yi(QE)	Cui Chaoyang
Zhao Yanli(PI)	Wang Zhihui
APPROVED	
Liu Xinghong(PM)	

Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

NV173FHM-N4F is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 17.3inch diagonally measured active area with Full-HD resolutions (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 8bit colors and color gamut DCI-P3 100%. The TFT-LCD panel used for this module is a low reflection and higher color type. Therefore, this module is suitable for Notebook PC. The LED driver for back-light driving is built in this model.

All input signals are eDP1.2 interface compatible.

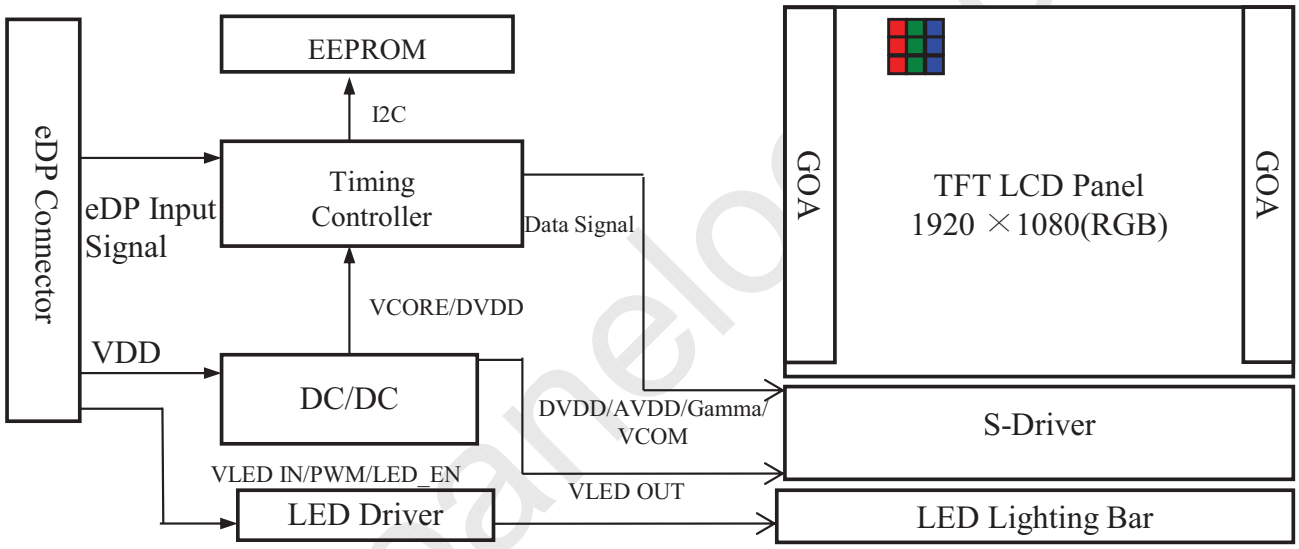


Figure 1. Drive Architecture

1.2 Features

- 2 lane eDP interface with 2.7Gbps link rates
- Thin and light weight
- 8bit color depth, color gamut DCI-P3 100%
- Single LED lighting bar (Bottom side/Horizontal Direction)
- Data enable signal mode
- Green product (RoHS & Halogen free product)
- On board LED driving circuit
- Low driving voltage and low power consumption
- On board EDID chip
- DPCD Version 1.1
- Function：SDRRS/CABC/BIST

1.3 Application

● Notebook PC (Wide type)

1.4 General Specification

The followings are general specifications at the model NV173FHM-N4F. (listed in Table 1)

<Table 1. General Specifications>

Parameter	Specification	Unit	Remarks
Active area	381.888(H) ×214.812(V)	mm	
Number of pixels	1920 (H) ×1080 (V)	pixels	
Pixel pitch	198.9(H) ×198.9(V)	um	
Pixel arrangement	RGB Vertical stripe		
Display colors	8bit		
Color gamut	DCI-P3 100%		
Display mode	Normally Black		
Dimensional outline	389.888±0.3(H)*238.312±0.5(V) (W/PCB)* 3.5(Max.) 389.888±0.3(H)*227.012±0.3(V) (W/O PCB)*3.3±0.2	mm	
Weight	500(Max.)	g	
Surface treatment	Anti-Glare		
Surface hardness	3H		
Back-light	Bottom edge side, 1-LED lighting bar type		Note 1
Power consumption	P_D : 0.8(Max.)	W	@Mosaic
	P_{BL} : 7.6(Max.)	W	
	P_{Total} : 8.4(Max.)	W	@Mosaic

Notes : 1. LED Lighting Bar (60*LED Array)

2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Absolute Maximum Ratings>

Ta=25+/-2°C

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-0.3	4.0	V	Note 1
eDP input Voltage	V_{eDP}	0	2.0	V	
Logic Supply Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V	
Operating Temperature	T_{OP}	0	+50	°C	Note 2
Storage Temperature	T_{ST}	-20	+60	°C	

Notes :
1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.
2. Temperature and relative humidity range are shown in the figure below.
95 % RH Max. (40 °C ≥ Ta) Maximum wet-bulb temperature at 39°C or less.(Ta >40°C)No condensation.

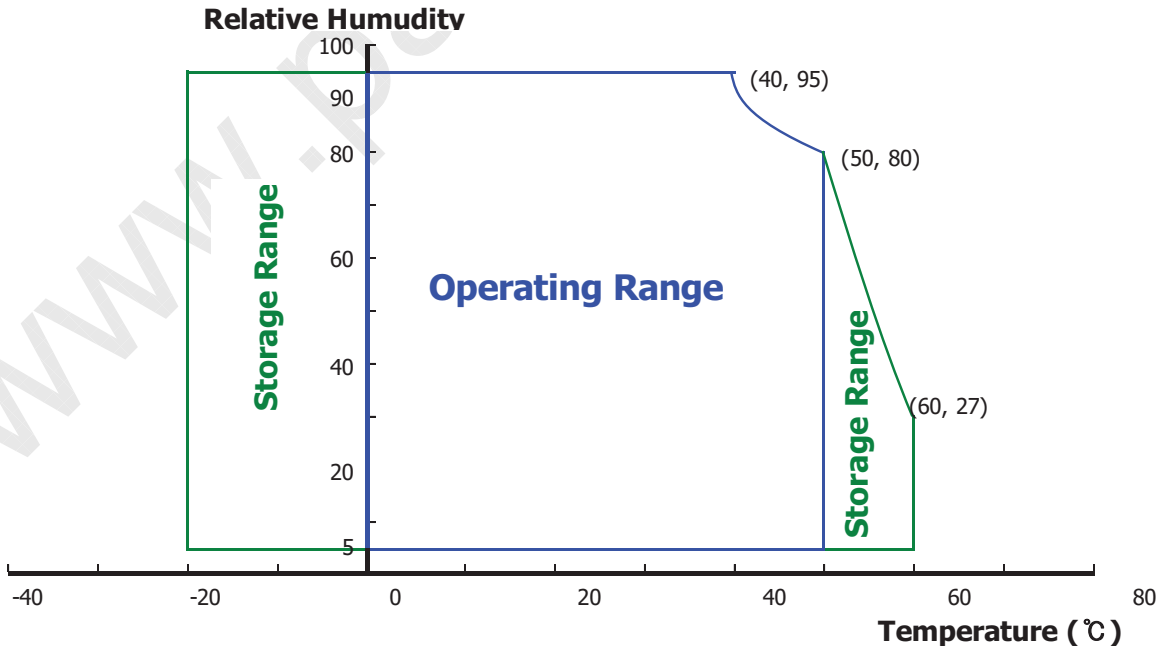


Figure 2. Temperature and Relative Humidity Range

3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

< Table 3. Electrical Specifications > Ta=25+/-2°C

Parameter			Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage		V_{DD}	3.0	3.3	3.6	V	Note 1
Permissible Input Ripple Voltage		V_{RF}	-10% VDD	-	+10% VDD	V	Note 4
CABC Control Level		High Level	2	-	3.6	V	Note 5
		Low Level	0	-	0.5	V	
BIST Control Level		High Level	2	-	3.6	V	
		Low Level	0	-	0.5	V	
Power Supply Inrush Current		Inrush	-	-	2	A	Note3
Power Supply Current	Mosaic	I_{DD}	-	-	242.4	mA	
	Red		-	-	424.2	mA	
	Green		-	-	424.2	mA	
	Blue		-	-	424.2	mA	
Power Consumption	Mosaic	P_M	-	-	0.8	W	
	Red	P_R	-	-	1.4	W	
	Green	P_G	-	-	1.4	W	
	Blue	P_B	-	-	1.4	W	
	BLU	P_{BL}	-	-	7.6	W	Note 2
	Total	P_{Total}	-	8.4	9	W	Note 1

3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

Notes :

1. The supply voltage is measured and specified at the interface connector of LCM.
   The current draw and power consumption specified is for 3.3V at 25 °C.(Typ. value for reference)
   a) Mosaic pattern 8*8
   b) R/G/B patterns

(a) (b)

Figure 3. Power Measure Patterns

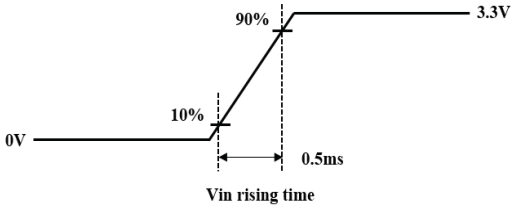


Figure 4. Inrush Measure Condition

2. Calculated value for reference ($V_{LED} \times I_{LED}$)
3. Measure condition (Figure 4)
4. Input voltage range:3.0~3.6V.Test condition: Oscilloscope bandwidth 20MHz, AC coupling
5. CABC&BIST setting

Pin No	Define	Enable	Disable
1	CABC	Pull High	Pull Low/Floating
14	BIST	Pull High	Pull Low/Floating

3.2 Backlight Unit

< Table 4. LED Driving Guideline Specifications > Ta=25+/-2°C

Parameter			Min.	Typ.	Max.	Unit	Remarks
LED Forward Voltage		V_F	-	-	5.65	V	
LED Forward Current		I_F	-	19.3	-	mA	
LED Power Input Voltage		V_{LED}	6	12	21	V	
LED Power Input Current		I_{LED}	-	-	633	mA	Note 1
LED Power Consumption		P_{LED}	-	-	7.6	W	
Power Supply Voltage for LED Driver Inrush		Iled inrush	-	-	1.5	A	
LED Life-Time		N/A	15,000	-	-	Hour	IF = 19.3mA Note 2
EN Control Level	Backlight On	V_{BL_EN}	2	-	3.6	V	Note 4
	Backlight Off		0	-	0.5	V	
PWM Control Level	High Level	V_{BL_PWM}	2	-	3.6	V	
	Low Level		0	-	0.5	V	
PWM Control Frequency		F_{PWM}	200	-	2,000	Hz	
Duty Ratio			5	-	100	%	Note 3

Notes :
1. The current and power consumption with LED Driver are under the VLED = 12.0V , 25℃, PWM Duty 100% .
2. The LED life-time define as the estimated time to 50% degradation of initial luminous.
3. Measure condition (Figure 5).
4.LED_EN&PWM setting

Pin No	Define	Enable	Disable
22	LED_EN	Pull High	Pull Low/Floating
23	PWM	Pull High	Pull Low/Floating

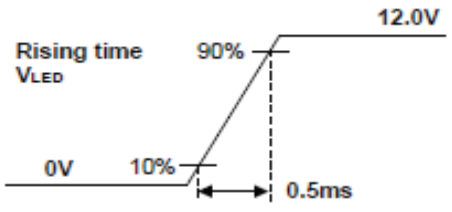


Figure 5. Inrush Measure Condition

3.3 LED Structure

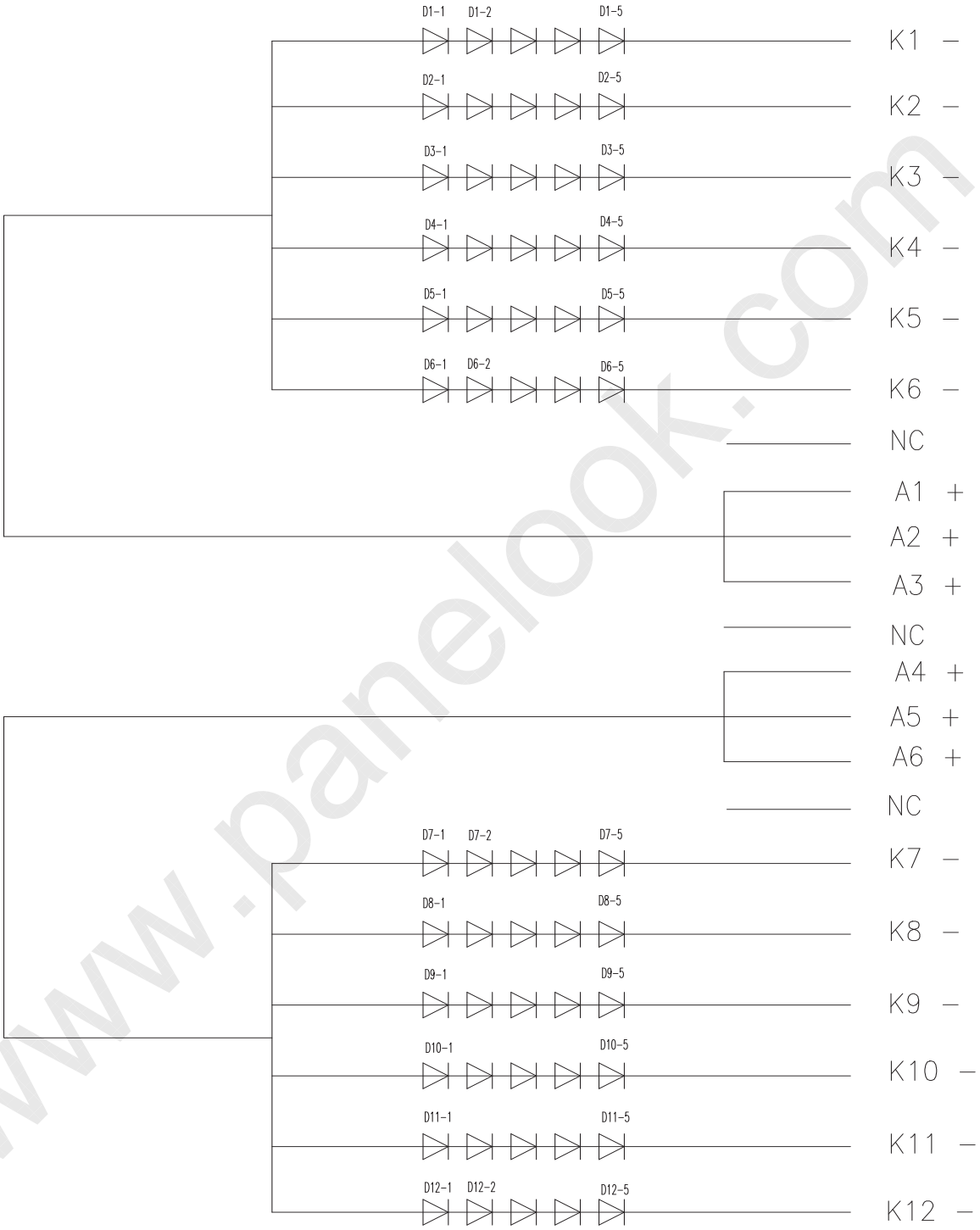


Figure 6. LED Structure

4.0 OPTICAL SPECIFICATION

4.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2℃) with the equipment of luminance meter system (PR730&PR810) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to θØ=0 (=θ3) as the 3 o'clock direction (the "right"), θØ=90 (= θ12) as the 12 o'clock direction ("upward"), θØ=180 (= θ9) as the 9 o'clock direction ("left") and θØ=270(= θ6) as the 6 o'clock direction ("bottom"). While scanning θand/or Ø, the center of the measuring spot on the display surface shall stay fixed. The backlight should be operating for 30 minutes prior to measurement. VDD shall be 3.3+/- 0.3V at 25°C. Optimum viewing angle direction is 6 'clock.

4.2 Optical Specifications

<Table 5. Optical Specifications>

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ_3	CR > 10	80	85	-	Deg.	Note 1
		Θ_9		80	85	-	Deg.	
	Vertical	Θ_{12}		80	85	-	Deg.	
		Θ_6		80	85	-	Deg.	
Luminance Contrast Ratio		CR	Θ = 0°	600	800	-		Note 2
Luminance of White	5 Points	Y_w	Θ = 0° I_{LED} = 19.3mA	425	500	-	cd/m²	Note 3
White Luminance Uniformity	5 Points	ΔY5		80	-	-		Note 4
	13 Points	ΔY13		65	-	-		
White Chromaticity		W_x	Θ = 0°	0.283	0.313	0.343		Note 5
		W_y		0.299	0.329	0.359		
Reproduction of Color	Red	R_x	Θ = 0°	Typ.-0.03	0.692	Typ.+0.03		
		R_y			0.318			
	Green	G_x			0.267			
		G_y			0.683			
	Blue	B_x			0.151			
		B_y			0.055			
Color Gamut				95	100	-	%	DCI-P3
Gamma Curve				2.0	2.2	2.4		
Response Time (Rising + Falling)		T_{RT}	Ta= 25℃ Θ = 0°	-	16	25	ms	Note 6
Cross Talk		CT	Θ = 0°	-	-	2.0	%	Note 7

Notes :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 7).

2. Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see Figure 7) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Center Luminance of white is defined as luminance values of 5 point average across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 8 for a total of the measurements per display.

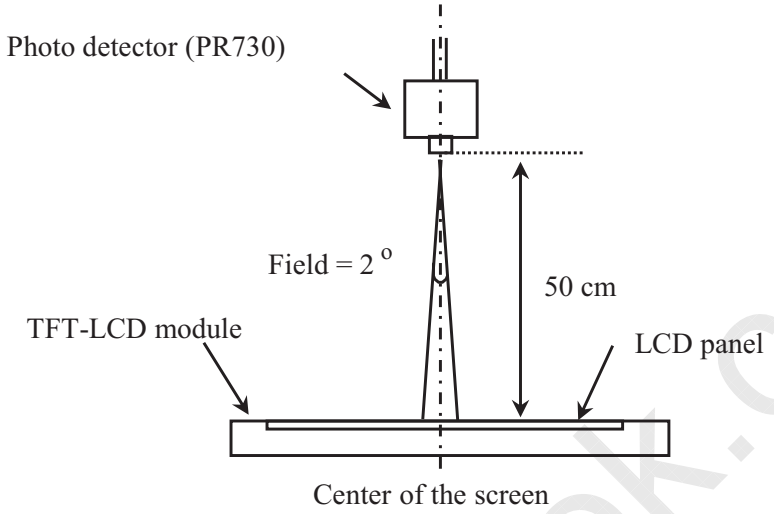
4. The White luminance uniformity on LCD surface is then expressed as : ΔY =Minimum Luminance of 5(or 13) points / Maximum Luminance of 5(or 13) points.(see Figure 8 and Figure 9).

5. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

6. The electro-optical response time measurements shall be made as Figure 10 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_r, and 90% to 10% is T_f.

7. Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (Y_A) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (Y_B) of that same area when any adjacent area is driven dark. (See Figure 11).

4.3 Optical Measurements



Optical characteristics measurement setup

Figure 7. Measurement Set Up

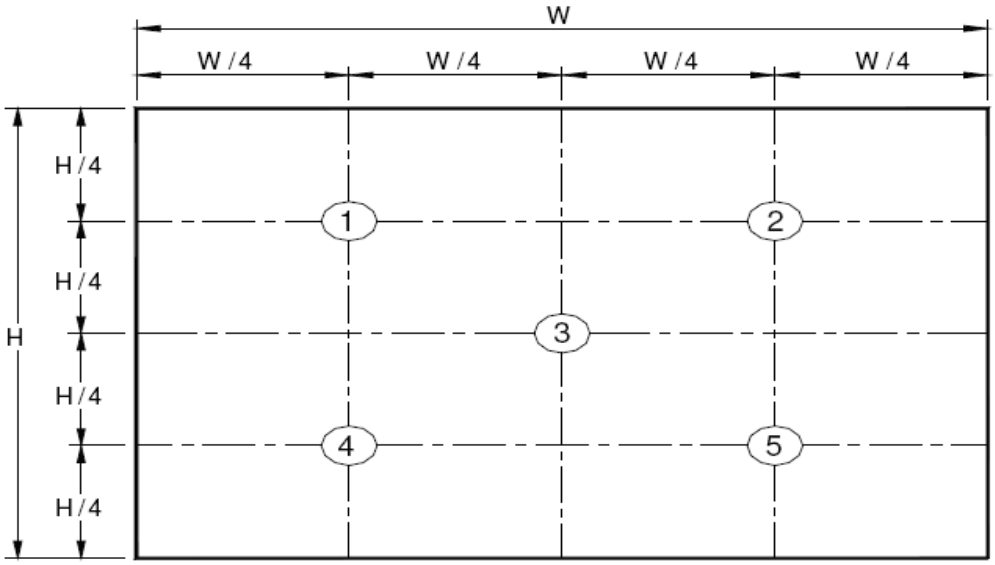


Figure 8. White Luminance and Uniformity Measurement Locations (5 points)

Center Luminance of white is defined as luminance values of center 5 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 7 for a total of the measurements per display.

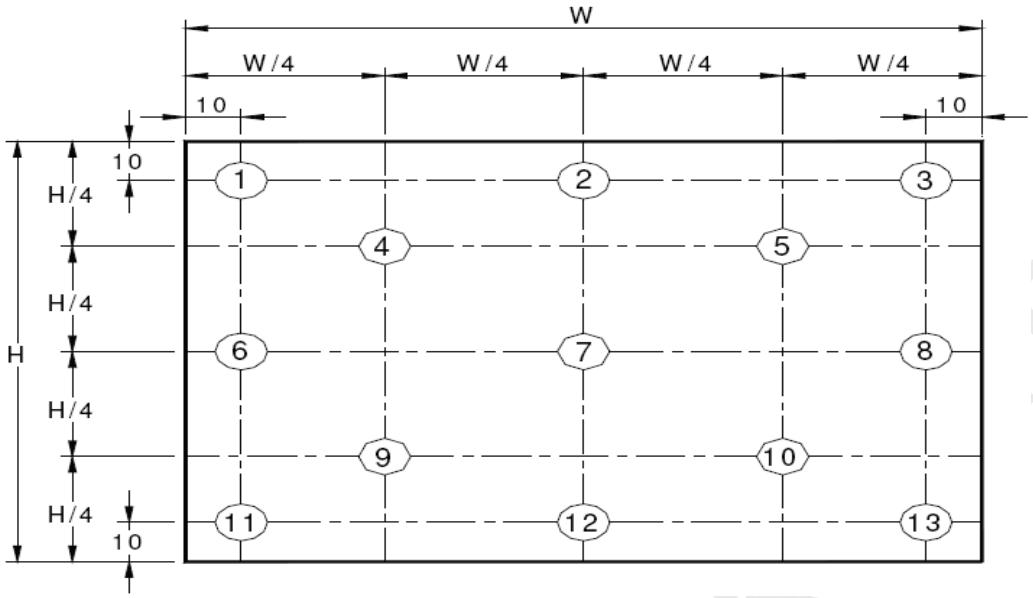


Figure 9. Uniformity Measurement Locations (13 points)

The White luminance uniformity on LCD surface is then expressed as : ΔY5 = Minimum Luminance of five points / Maximum Luminance of five points (see Figure 8) , ΔY13 = Minimum Luminance of 13 points /Maximum Luminance of 13 points (see Figure 9).

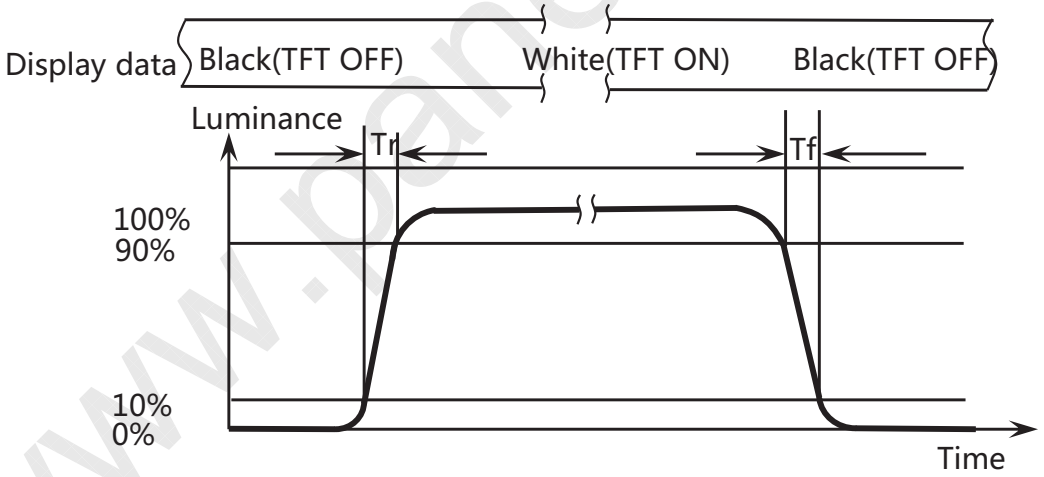
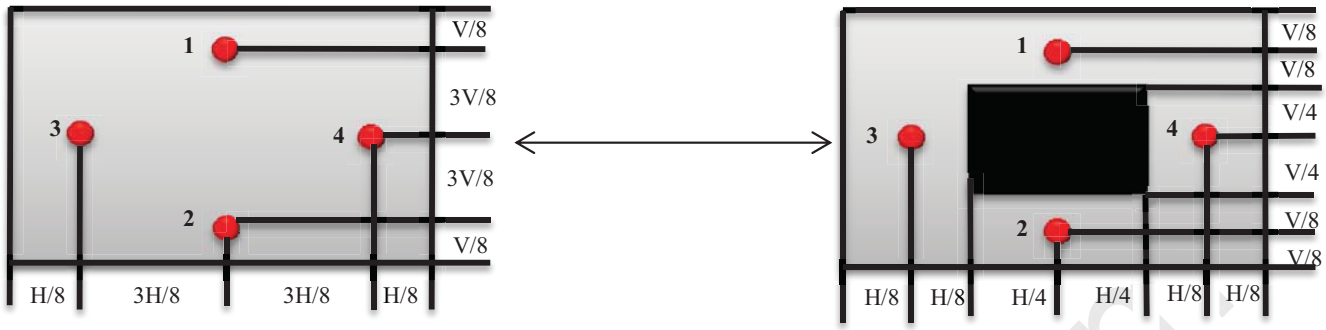


Figure 10. Response Time Testing

The electro-optical response time measurements shall be made as shown in Figure 10 by switching the "data" input signal ON and OFF. Tr: The luminance to change from 10% to 90% ,Tf: The luminance to change from 90% to 10% .

The test system : LMS PR810



$$\text{Cross Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_A} \right| \times 100$$

Figure 11. Cross Talk Modulation Test Description

Where:

Y_A = Initial luminance of measured area (cd/m^2)

Y_B = Subsequent luminance of measured area (cd/m^2)

The location 1/2/3/4 measured will be exactly the same in both patterns. The test background gray is from L64 to L192.Take the largest data as the result.

Cross Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark.(Refer to Figure 11)

The test system: PR730

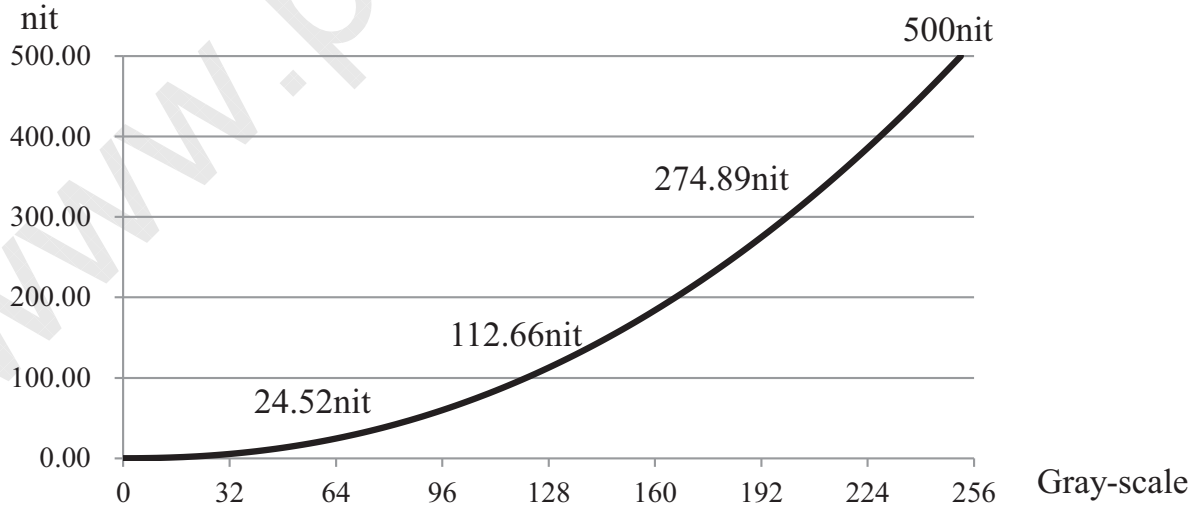


Figure 12. Brightness and Gray-scale Contrast

5.0 INTERFACE CONNECTION

5.1 Electrical Interface Connection

The electronics interface connector is STM MSAK24025P30 or Compatible.
The connector interface pin assignments are listed in Table 6.

<Table 6. Pin Assignments for the Interface Connector>

Pin No.	Symbol	Description
1	CABC_EN	CABC_Function Reserved
2	H_GND	Ground
3	LANE1_N	eDP RX Channel 1 Negative
4	LANE1_P	eDP RX Channel 1 Positive
5	H_GND	Ground
6	LANE0_N	eDP RX Channel 0 Negative
7	LANE0_P	eDP RX Channel 0 Positive
8	H_GND	Ground
9	AUX_CH_P	eDP AUX CH Positive
10	AUX_CH_N	eDP AUX CH Negative
11	H_GND	Ground
12	LCD_VCC	Power Supply, 3.3V (typ.)
13	LCD_VCC	Power Supply, 3.3V (typ.)
14	BIST	Panel Self Test Enable
15	H_GND	Ground
16	H_GND	Ground
17	HPD	Hot Plug Detect Output
18	BL_GND	LED Ground
19	BL_GND	LED Ground
20	BL_GND	LED Ground
21	BL_GND	LED Ground
22	BL_ENABLE	LED Enable Pin(+3.3V Input)
23	BL_PWM	System PWM Signal Input
24	NC	No Connection
25	NC	No Connection
26	BL_POWER	LED Power Supply 6V-21V
27	BL_POWER	LED Power Supply 6V-21V
28	BL_POWER	LED Power Supply 6V-21V
29	BL_POWER	LED Power Supply 6V-21V
30	NC	No Connection

5.2 eDP Interface

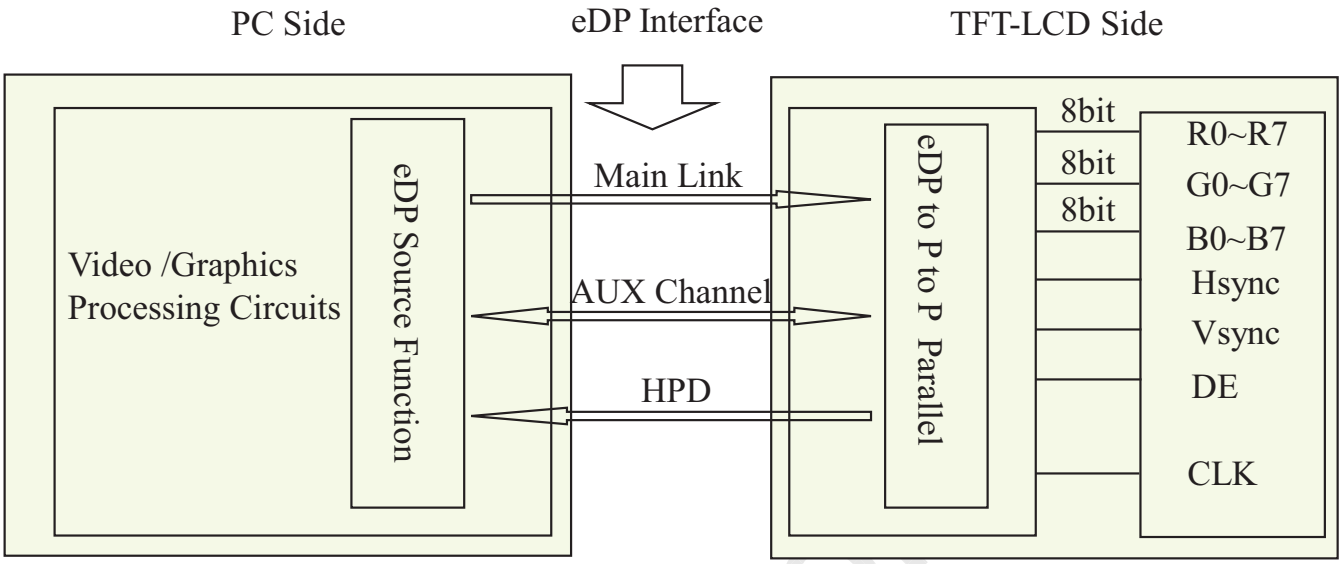


Figure 13. eDP Interface Architecture

Note:
Transmitter : Parade DP501 or equivalent.
Transmitter is not contained in module.

5.3 Data Input Format

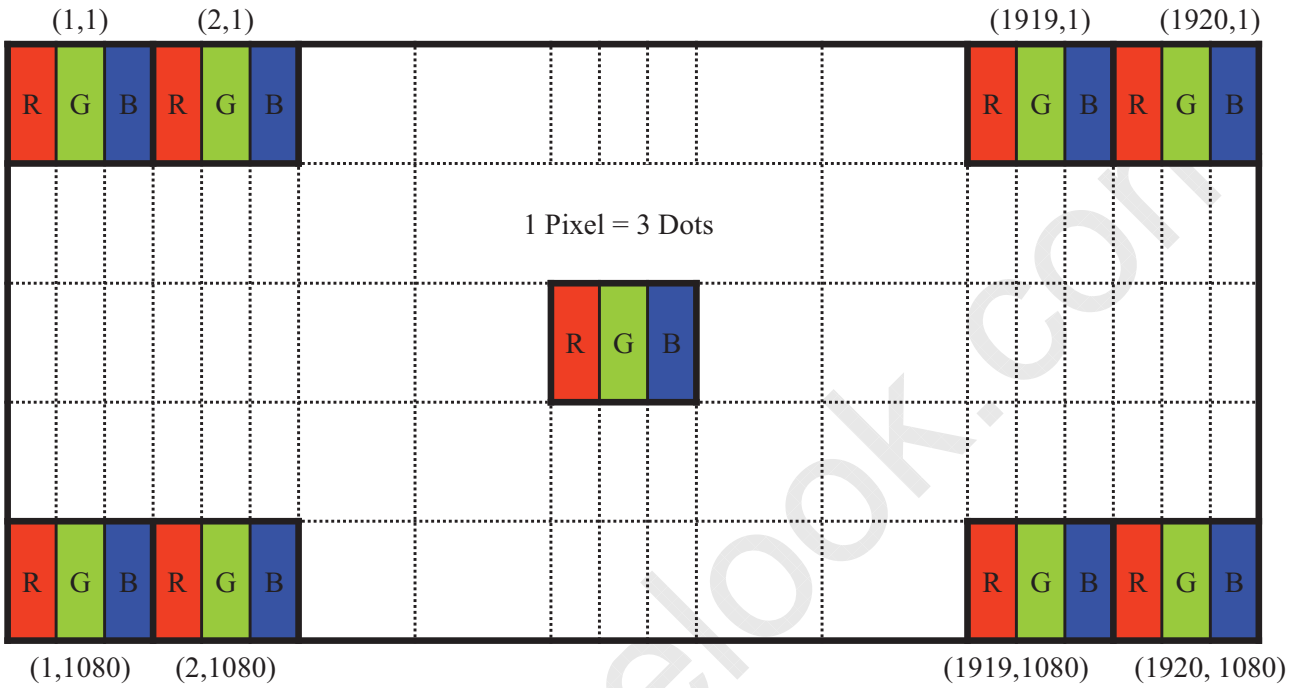


Figure 14. Display Position of Input Data (V-H)

5.4 Back-light & LCM Interface Connection

BLU Interface Connector: I-PEX 20599-021E-01 or Compatible.

<Table 7. Pin Assignments for the BLU Connector>

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	LED	LED cathode connection	12	Vout	LED anode connection
2	LED	LED cathode connection	13	Vout	LED anode connection
3	LED	LED cathode connection	14	Vout	LED anode connection
4	LED	LED cathode connection	15	NC	No Connection
5	LED	LED cathode connection	16	LED	LED cathode connection
6	LED	LED cathode connection	17	LED	LED cathode connection
7	NC	No Connection	18	LED	LED cathode connection
8	Vout	LED anode connection	19	LED	LED cathode connection
9	Vout	LED anode connection	20	LED	LED cathode connection
10	Vout	LED anode connection	21	LED	LED cathode connection
11	NC	No Connection			

6.0 SIGNAL TIMING SPECIFICATION

6.1 The NV173FHM-N4F Is Operated By The DE Only

< Table 8. Signal Timing Specification >

Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	143.4	147.8	152.2	MHz
Frame Period		Tv	1103	1120	1136	lines
			-	60	-	Hz
			-	16.67	-	ms
Vertical Display Period		Tvd	-	1080	-	lines
One line Scanning Period		Th	2167	2200	2233	clocks
Horizontal Display Period		Thd	-	1920	-	clocks

Note : The above is as optimized setting.

6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 9.

<Table 9. eDP Main-Link RX TP4 Package Pin Parameters>

Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock (Link clock down-spreading)	SSC	0	-	0.5	%	
Differential peak-to-peak input voltage at package pins	$V_{RX-DIFFp-p}$	100	-	1320	mV	
Rx input DC common mode voltage	$V_{RX\_DC\_CM}$	0	-	2	V	
Differential termination resistance	$R_{RX-DIFF}$	80	100	120	Ω	
Single-ended termination resistance	R_{RX-SE}	40	-	60	Ω	
Rx short circuit current limit	I_{RX_SHORT}	-	-	20	mA	
Intra-pair skew at Rx package pins (HBR) RX intra-pair skew tolerance at HBR	$L_{RX\_SKEW\_INTRA\_PAIR}$	-	-	150	ps	
AC Coupling Capacitor	C_{SOURCE_ML}	75	-	200	nF	Source side

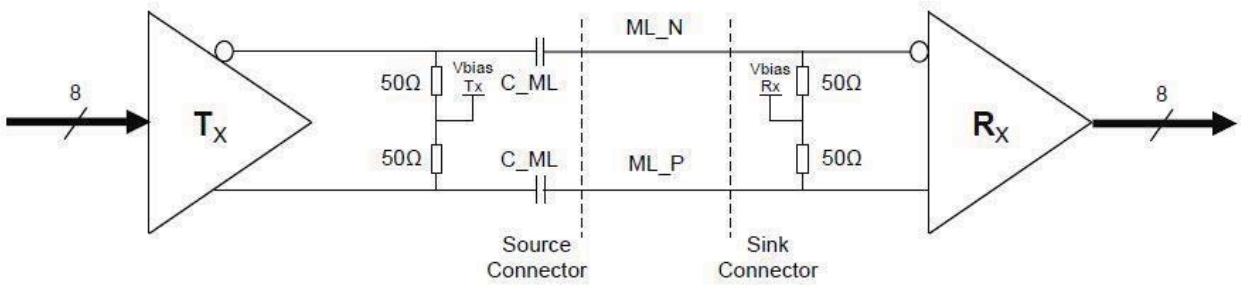


Figure 15. Main link differential pair

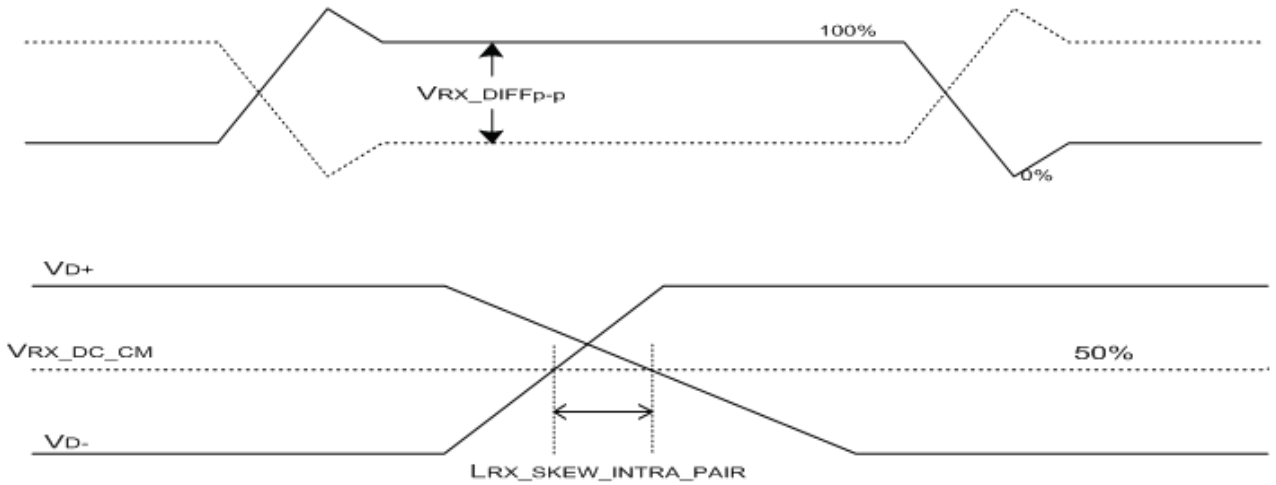


Figure 16. VRX-DIFFp-p & LRX_SKEW_INTRA_PAIR

<Table 10. HPD Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
HPD voltage	V_{HPD}	2.25	-	2.75	V	Sink side
Hot Plug Detection Threshold	-	2	-	-	V	Source side
Hot Unplug Detection Threshold	-	-	-	0.3	V	
HPD_IRQ Pulse Width	HPD_IRQ	0.5	-	1	ms	
HPD_TimeOut	-	2.0	-	-	ms	

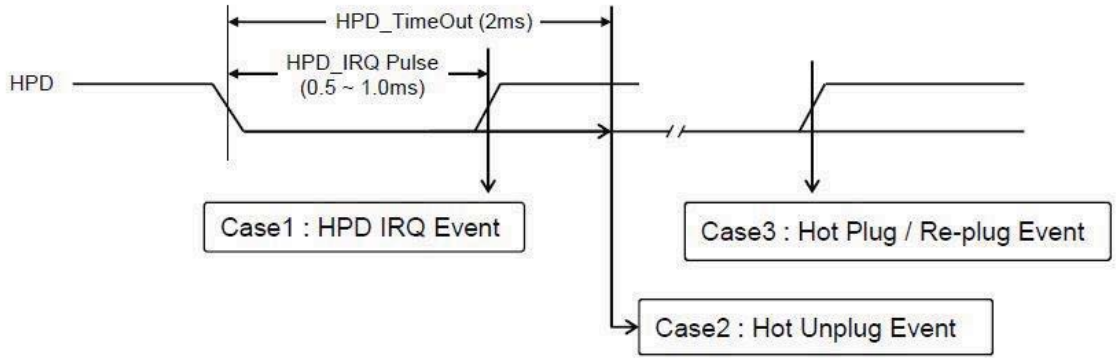


Figure 17. HPD Events

<Table 11. AUX Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
AUX unit interval	U_{IAUX}	0.4	0.5	0.7	Us	
AUX peak-to-peak input differential voltage	$V_{AUX-RX-DIFFp-p}$	0.18	-	0.8	V	Sink Side Connector Pin
AUX CH termination DC resistance	$R_{AUX-TERM}$	80	100	120	Ohm	
AUX DC common mode voltage	$V_{AUX-DC-CM}$	0	-	2	V	
AUX turn around common mode voltage	$V_{AUX-TURN-CM}$	-	-	0.3	V	
AUX short circuit current limit	$I_{AUX-SHORT}$	-	-	20	mA	
AUX AC Coupling Capacitor	$C_{SOURCE-AUX}$	75	-	200	nF	Source side

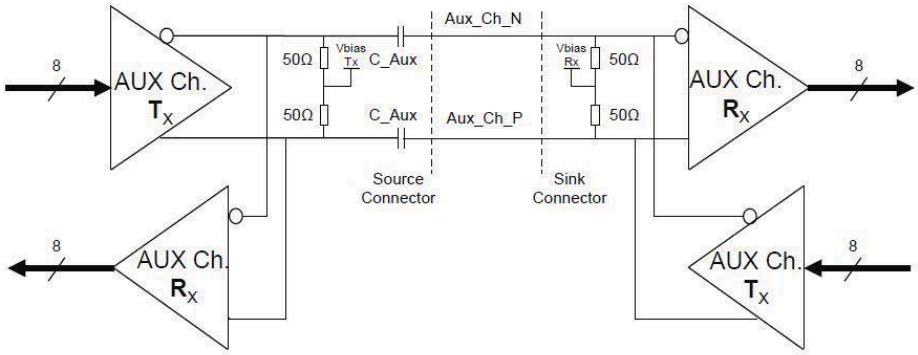


Figure 18. AUX differential pair

7.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

<Table 12. Input Signal & Basic Display Colors & Gray Scale of Colors >

	Colors & Gray scale	Data signal		
		R0 R1 R2 R3 R4 R5 R6 R7	G0 G1 G2 G3 G4 G5 G6 G7	B0 B1 B2 B3 B4 B5 B6 B7
Basic colors	Black	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	Blue	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1
	Green	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0
	Light Blue	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
	Red	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	Purple	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1
	Yellow	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0
	White	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
Gray scale of Red	Black	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	△	1 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	Darker	0 1 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	△	↑	↑	↑
	▽	↓	↓	↓
	Brighter	1 0 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	▽	0 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	Red	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Gray scale of Green	Black	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	△	0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	Darker	0 0 0 0 0 0 0 0	0 1 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	△	↑	↑	↑
	▽	↓	↓	↓
	Brighter	0 0 0 0 0 0 0 0	1 0 1 1 1 1 1 1	0 0 0 0 0 0 0 0
	▽	0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0
	Green	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0
Gray scale of Blue	Black	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	△	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0
	Darker	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 1 0 0 0 0 0 0
	△	↑	↑	↑
	▽	↓	↓	↓
	Brighter	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 0 1 1 1 1 1 1
	▽	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1
	Blue	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1
Gray scale of White& Black	Black	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	△	1 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0
	Darker	0 1 0 0 0 0 0 0	0 1 0 0 0 0 0 0	0 1 0 0 0 0 0 0
	△	↑	↑	↑
	▽	↓	↓	↓
	Brighter	1 0 1 1 1 1 1 1	1 0 1 1 1 1 1 1	1 0 1 1 1 1 1 1
	▽	0 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1
	White	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1

8.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below.

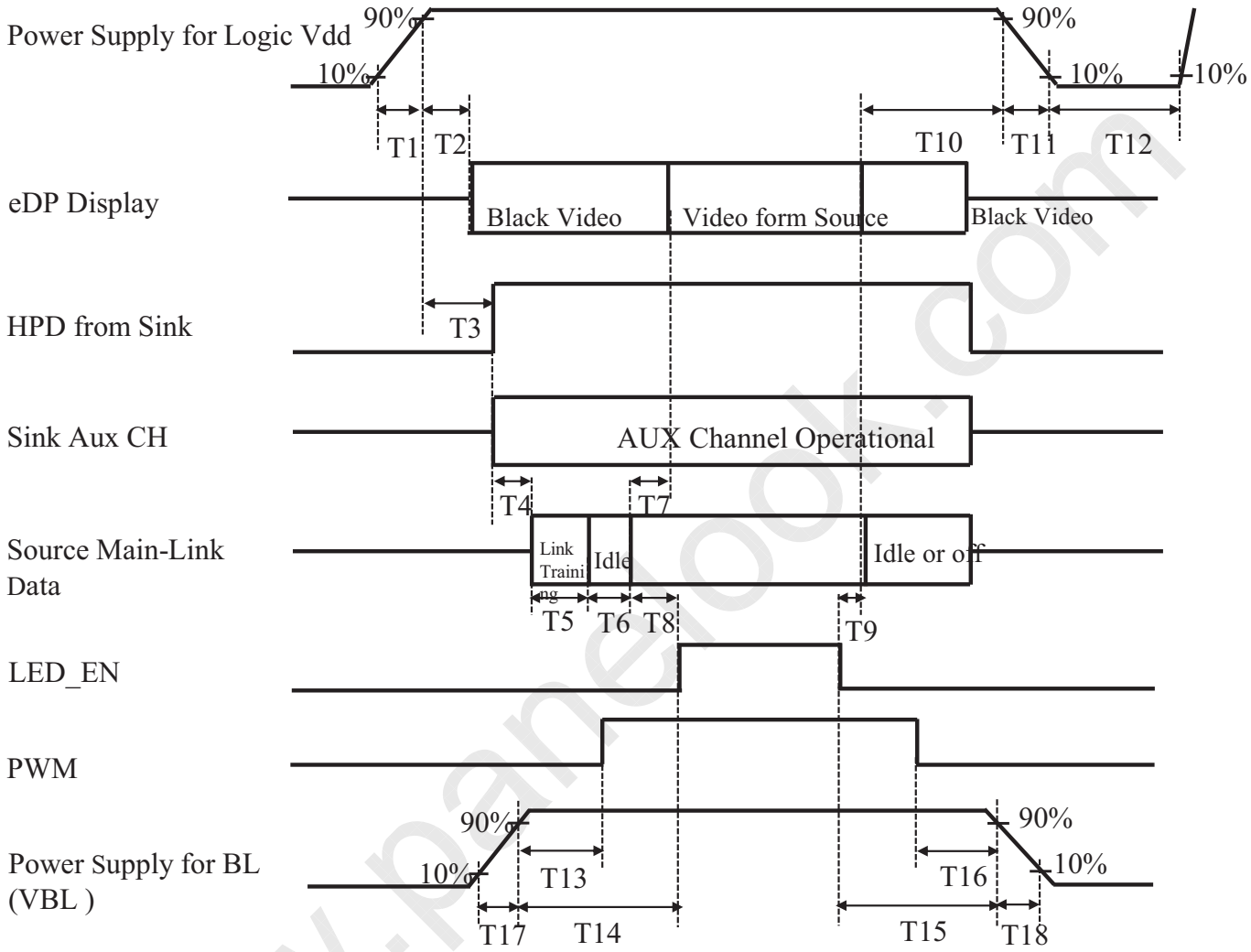


Figure 19. Power Sequence

- 0.5ms ≤ T1 ≤ 10 ms
- 0ms < T2 ≤ 200 ms
- 0ms < T3 ≤ 200 ms
- T3+T4+T5+T6+T8>200ms
- 0ms < T7 ≤ 50ms
- 50ms < T8
- 0ms < T9
- 0ms < T10 < 500 ms
- 0.5ms ≤ T11 ≤ 10 ms
- 500ms ≤ T12
- 0ms < T13
- 0ms < T14
- 0ms < T15
- 0ms < T16
- 0.5ms ≤ T17
- 0.5ms ≤ T18

Notes:

1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal are valid.

9.0 Connector Description

Physical interface is described as for the connector on LCM.
These connectors are capable of accommodating the following signals and will be following components.

9.1 TFT LCD Module

< Table 13. Signal Connector >

Connector Name /Description	For Signal Connector
Manufacturer	STM or Compatible
Type/ Part Number	STM MSAK24025P30 or Compatible
Mating Housing/ Part Number	I-PEX 20455-030E or Compatible

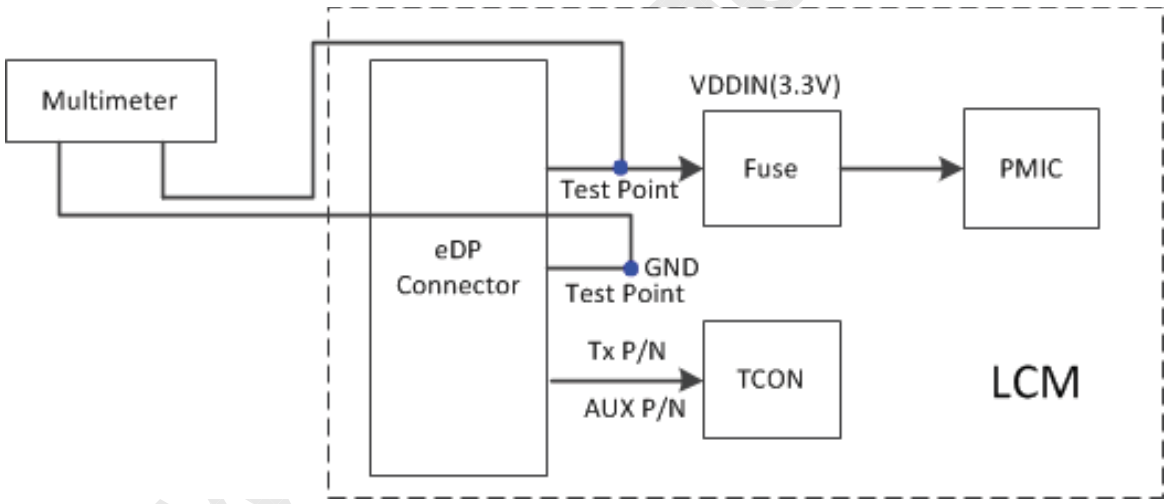
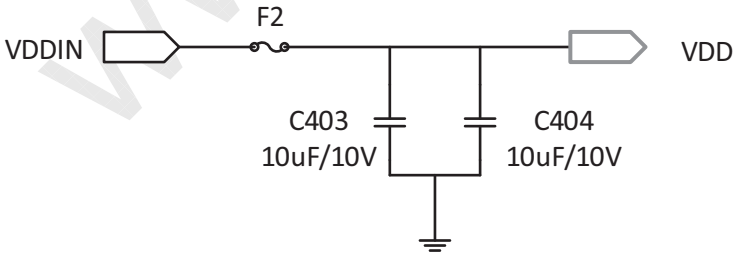


Figure 20. RC Loading Test Schematic Diagram



Item	RC Loading	
VC9PN	R	C
	10.13KΩ	32nF

Figure 21. VCC Loop R/C Loading Parameter

10.0 MECHANICAL CHARACTERISTICS

10.1 Dimensional Requirements

Figure 26 shows mechanical outlines for the model NV173FHM-N4F.
Other parameters are shown in Table 14.

<Table 14. Dimensional Parameters>

Parameter	Specification	Unit
Active Area	381.888(H) ×214.812(V)	mm
Number of pixels	1920 (H) ×1080 (V)	pixels
Pixel pitch	198.9(H) ×198.9(V)	um
Pixel arrangement	RGB Vertical stripe	
Display colors	8bit	
Display mode	Normally Black	
Dimensional outline	389.888±0.3(H)*238.312±0.5(V) (W/PCB)*3.5(Max.) 389.888±0.3(H)*227.012±0.3(V) (W/O PCB)*3.3±0.2	mm
Weight	500(Max.)	g

10.2 Mounting

See Figure 26.

10.3 Anti-Glare and Polarizer Hardness.

The surface of the LCD has an Anti-Glare coating to minimize reflection and a coating to reduce scratching. The polarizer hardness is 3H.

10.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 350lux.

11.0 RELIABILITY TEST

The reliability test items and its conditions are shown in below.

<Table 15. Reliability Test>

No	Test Items	Conditions	Remark
1	High temperature storage test	Ta = 60˚C , 60%RH, 240 hrs	
2	Low temperature storage test	Ta = -20˚C , 240 hrs	
3	High temperature & high humidity operation test	Ta = 50˚C , 80%RH, 240 hrs	
4	High temperature operation test	Ta = 50˚C , 60%RH, 240 hrs	
5	Low temperature operation test	Ta = 0˚C , 240 hrs	
6	Thermal shock	Ta = -20 ˚C ↔ 60 ˚C (0.5 hr), 60%±3%RH, 100 cycle	
7	Vibration test (non-operating)	Ta = 25˚C , 60%RH, 1.5G, 10~500Hz, Sine X,Y,Z / Sweep rate : 1 hour	Note 1
8	Shock test (non-operating)	Ta = 25˚C , 60%RH, 220G, Half Sine Wave 2msec ±X, ±Y, ±Z Once for each direction	Note 1
9	Electro-static discharge test (operating)	Air : 150 pF, 330Ω, ±15 KV Contact : 150 pF, 330Ω, ±8 KV Ta = 25˚C , 60%RH,	Note 2

Notes :

1. The fixture must be hard enough , so that the module would not be twisted or bent.
2. Self- recovery and restart recovery is allowed. No hardware failures.

12.0 HANDLING & CAUTIONS

(1) Cautions when taking out the module
- Pick the pouch only, when taking out module from a shipping package.

(2) Cautions for handling the module
- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation
- When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

(4) Cautions for the atmosphere
- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics
- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions
- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc. Please pack the module not to be broken. We recommend to use the original shipping packages.

13.0 LABEL

(1) Product Label

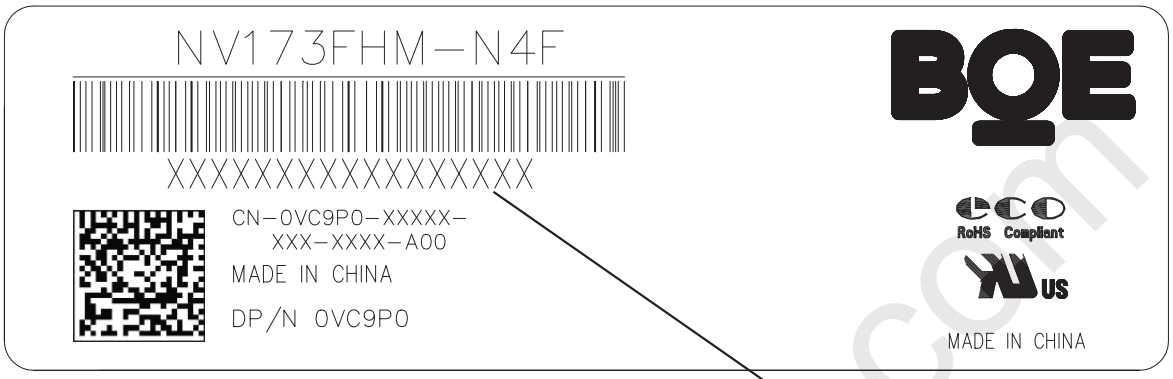


Figure 22. Product Label

Module ID Naming Rule:

<Table 16. Module ID Naming Rule>

Digit / Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Code	B	9	A	F	1	7	8	8	D	3	1	0	0	0	0	6	8
Description	Product Name		Product Grade	B8	Year		Month	Model Extension Code (Last 4 Digits of FG CODE)				Serial No. 00001-ZZZZZZ					

(2) High voltage caution label

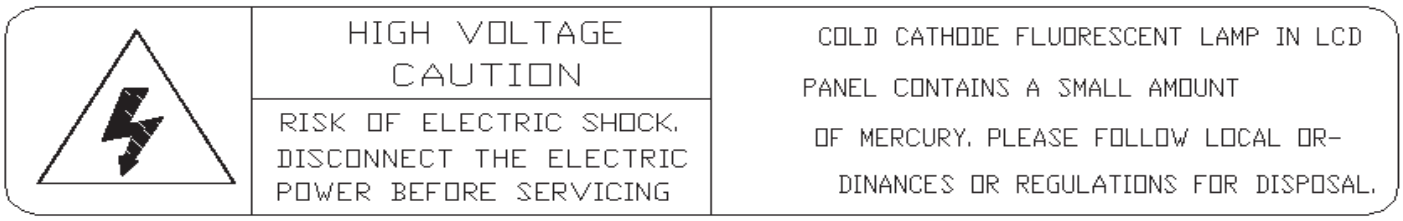


Figure 23. High Voltage Caution Label

(3) Box label

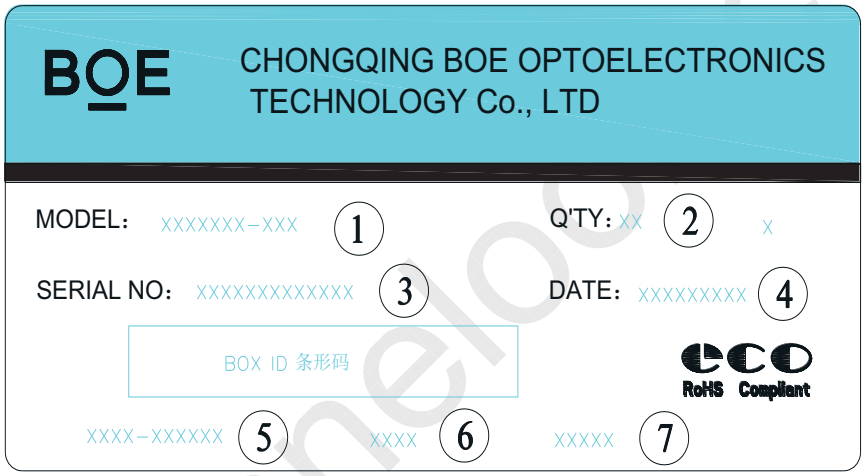


Figure 24. Box Label

Serial number marked part needs to print, show as follows:

1. FG-CODE(Before 12 bit)
2. Product quantity
3. Box ID
4. Date
5. The client section material number(The client)
6. FG-Code After four
7. The supplier code

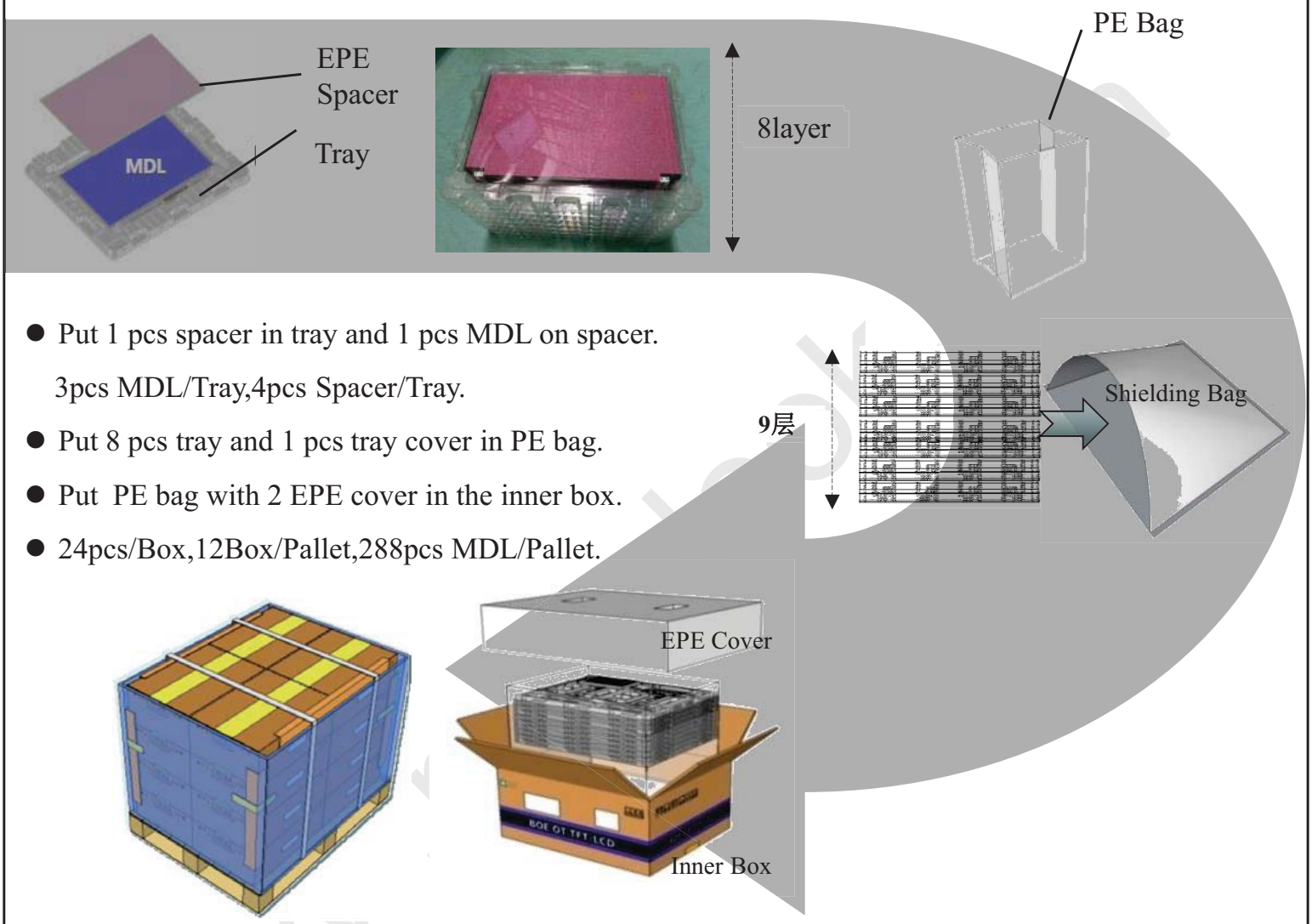
Total Size:100×50mm

<Table 17. Box Label Naming Rule >

Digit / Code	1	2	3	4	5	6	7	8	9	10	11	12	13
Code	B	9	A	F	1	7	8	N	0	0	3	2	7
Description	Product Name		Product Grade	B8	Year		Month	Revision	BOX Serial Number				

14.0 PACKING INFORMATION

14.1 Packing Order



- Put 1 pcs spacer in tray and 1 pcs MDL on spacer.
  3pcs MDL/Tray,4pcs Spacer/Tray.
- Put 8 pcs tray and 1 pcs tray cover in PE bag.
- Put PE bag with 2 EPE cover in the inner box.
- 24pcs/Box,12Box/Pallet,288pcs MDL/Pallet.

Figure 25. Packing Order

14.2 Note

- Box dimension: 522mm*392mm*294mm
- Package quantity in one box: 24pcs
- Total weight: 15.48kg/Box

15.0 MECHANICAL OUTLINE DIMENSION

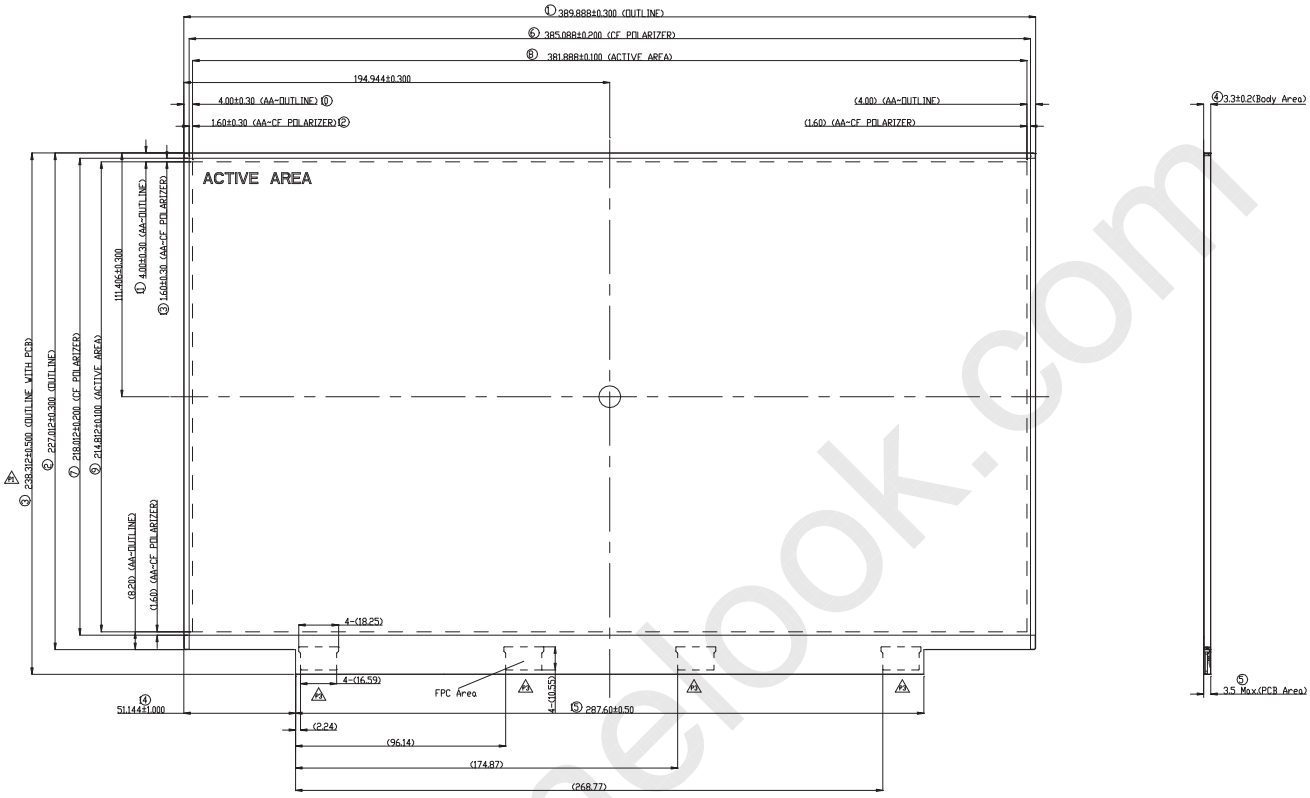


Figure 26. TFT-LCD Module Outline Dimension (Front View)

NOTES:
1.WARPAGE AND DEFORMATION SPEC.: 0.5mm MAX.
2.THE eDP CONNECTOR IS MEASURED AT PIN 1 AND MATING LINE
3.UNSPECIFIED TOLERANCE REFER TO `0.3 mm
4.THE MEASUREMENT METHOD FOR THE DIMENSION OF MODULE, PLEASE REFRE TO APPENDIX A.
5.TOP POLARIZER IS THE HIGHEST PORTION.
6."()" MEANS REFERANCE DIMENSIONS.
7.CRITICAL DIMENSION: 1-17
CPK: 1-4

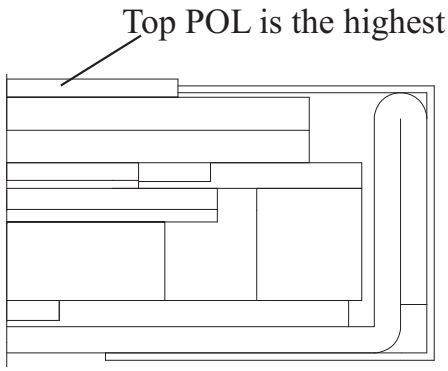


Figure 27. Highest Point Position

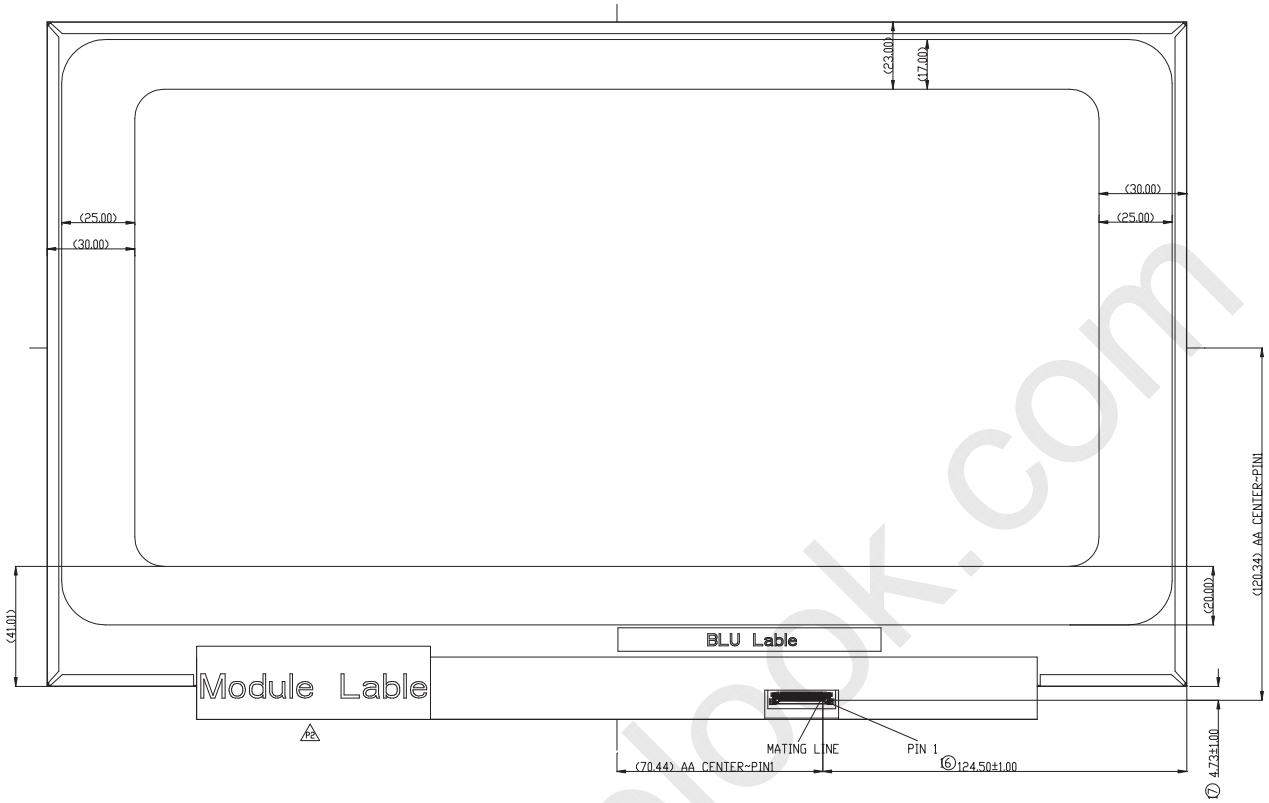


Figure 28. TFT-LCD Module Outline Dimensions (Rear view)

NOTES:
1.WARPAGE AND DEFORMATION SPEC.: 0.5mm MAX.
2.THE eDP CONNECTOR IS MEASURED AT PIN 1 AND MATING LINE
3.UNSPECIFIED TOLERANCE REFER TO ’0.3 mm
4.THE MEASUREMENT METHOD FOR THE DIMENSION OF MODULE, PLEASE REFRE TO APPENDIX A.
5.TOP POLARIZER IS THE HIGHEST PORTION.
6."()" MEANS REFERANCE DIMENSIONS.
7.CRITICAL DIMENSION:1-17
CPK:1-4

16.0 EDID Table

Address (HEX)	Function	Hex	Dec	Input values	Notes
00	Header	00	0	0	EDID Header
01		FF	255	255	
02		FF	255	255	
03		FF	255	255	
04		FF	255	255	
05		FF	255	255	
06		FF	255	255	
07		00	0	0	
08	ID Manufacturer Name	09	9	BOE	ID = BOE
09		E5	229		
0A	ID Product Code	C5	197	2245	ID = 2245
0B		08	8		
0C	32-bit serial No.	00	0	0	
0D		00	0	0	
0E		00	0	0	
0F		00	0	0	
10	Week of manufacture	24	36	36	
11	Year of Manufacture	1D	29	2019	Manufactured in 2019
12	EDID Structure Ver.	01	1	1	EDID Ver 1.0
13	EDID revision #	04	4	4	EDID Rev. 0.4
14	Video input definition	A5	165	-	Video Signal Interface
15	Max H image size	26	38	38	38cm (Approx)
16	Max V image size	15	21	21	21cm (Approx)
17	Display Gamma	78	120	2.2	Gamma curve = 2.2
18	Feature support	02	2	-	Feature Support
19	Red/Green low bits	67	103	-	Red / Green Low Bits
1A	Blue/White low bits	C5	197	-	Blue / White Low Bits
1B	Red x high bits	B1	177	0.692	Red (x) = 10110001 (0.692)
1C	Red y high bits	51	81	0.318	Red (y) = 01010001 (0.318)
1D	Green x high bits	44	68	0.267	Green (x) = 01000100 (0.267)
1E	Green y high bits	AE	174	0.683	Green (y) = 10101110 (0.683)
1F	Blue x high bits	26	38	0.151	Blue (x) = 00100110 (0.151)
20	BLue y high bits	0E	14	0.055	Blue (y) = 00001110 (0.055)
21	White x high bits	50	80	0.313	White (x) = 01010000 (0.313)
22	White y high bits	54	84	0.329	White (y) = 01010100 (0.329)
23	Established timing 1	00	0	-	--
24	Established timing 2	00	0	-	
25	Established timing 3	00	0	-	

26	Standard timing #1	01	1	-	Not Used
27		01	1	-	
28	Standard timing #2	01	1	-	Not Used
29		01	1	-	
2A	Standard timing #3	01	1	-	Not Used
2B		01	1	-	
2C	Standard timing #4	01	1	-	Not Used
2D		01	1	-	
2E	Standard timing #5	01	1	-	Not Used
2F		01	1	-	
30	Standard timing #6	01	1	-	Not Used
31		01	1	-	
32	Standard timing #7	01	1	-	Not Used
33		01	1	-	
34	Standard timing #8	01	1	-	Not Used
35		01	1	-	
36	Detailed timing/monitor descriptor #1	C0	192	147.84	147.84MHz Main clock
37		39	57		
38		80	128	1920	Hor Active = 1920
39		18	24	280	Hor Blanking = 280
3A		71	113	-	4 bits of Hor. Active + 4 bits of Hor. Blanking
3B		38	56	1080	Ver Active = 1080
3C		28	40	40	Ver Blanking = 40
3D		40	64	-	4 bits of Ver. Active + 4 bits of Ver. Blanking
3E		30	48	48	Hor Sync Offset = 48
3F		20	32	32	H Sync Pulse Width = 32
40		36	54	3	V sync Offset = 3 line
41		00	0	6	V Sync Pulse width : 6 line
42		7E	126	382	Horizontal Image Size = 382 mm (Low 8 bits)
43		D7	215	215	Vertical Image Size = 215 mm (Low 8 bits)
44		10	16	-	4 bits of Hor Image Size + 4 bits of Ver Image Size
45		00	0	0	Hor Border (pixels)
46		00	0	0	Vertical Border (Lines)
47		1A	26	-	Detailed timing Definition

48	Detailed timing/monitor descriptor #2	34	52	118.27	118.27MHz Main clock
49		2E	46		
4A		80	128	1920	Hor Active = 1920
4B		18	24	280	Hor Blanking = 280
4C		71	113	-	4 bits of Hor. Active + 4 bits of Hor. Blanking
4D		38	56	1080	Ver Active = 1080
4E		28	40	40	Ver Blanking = 40
4F		40	64	-	4 bits of Ver. Active + 4 bits of Ver. Blanking
50		30	48	48	Hor Sync Offset = 48
51		20	32	32	H Sync Pulse Width = 32
52		36	54	3	V sync Offset = 3 line
53		00	0	6	V Sync Pulse width : 6 line
54		7E	126	382	Horizontal Image Size = mm (Low 8 bits)
55		D7	215	215	Vertical Image Size = mm (Low 8 bits)
56		10	16	-	4 bits of Hor Image Size + 4 bits of Ver Image Size
57		00	0	0	Hor Border (pixels)
58		00	0	0	Vertical Border (Lines)
59		1A	26	-	Detailed timing Definition
5A	Detailed timing/monitor descriptor #3	00	0	-	ASCII Data Sting Tag
5B		00	0	-	
5C		00	0	-	
5D		FE	254	-	
5E		00	0	-	
5F		56	86	V	Dell P/N:VC9P0
60		43	67	C	
61		39	57	9	
62		50	80	P	
63		30	48	0	
64		80	128	10000000	EDID:A00
65		4E	78	N	BOE PN
66		56	86	V	
67		31	49	1	
68		37	55	7	
69		4E	78	N	
6A		34	52	4	
6B		46	70	F	

6C	Detailed timing/monitor descriptor #4	00	0	-	Flag
6D		00	0	-	
6E		00	0	-	
6F		00	0	-	Data Type Tag: Manufacturer Specified Data 00
70		00	0	-	Flag
71		02	2	-	Color Depth：8bit +2 bit FRC：No Supports
72		41	65	-	Lamps of LED Light Bars：one Configuration：single light bar Panel Illumination：WLED
73		21	33	-	Intel sDRRS：Supports Intel DRRS：No Supports Max. Frame Rate：65Hz Min. Frame Rate：40Hz
74		B2	178	-	Digatle/PWM：PWM only Maximum Typical Luminance：500
75		00	0	-	Pixel Structure：RGB v-strip Transflective：no AG/Glossy：Anti-Glare
76		10	16	-	Bynamic Backlight Control：DBC type 1 Color Management：NTSC
77		00	0	-	Active Gamma Control：no support(default) Montion Blur：no support(default)
78		00	0	-	In-Cell Scanner：no support(default) Wireless Enhancement Hardware：no support(default)
79		0A	10	-	In-Cell Touch：no support(default) Interface：eDP Overdrive：no support(default) Interface Channels：two
7A		01	1	-	3-D Hardware Support：no support(default) Electronic Privacy：no electronic privacy hardware control BIST Hardware support：support(default)
7B		0A	10	-	Format: terminate with ASCII code 0Ah and pad field with ASCII code 20h
7C		20	32	-	
7D		20	32	-	
7E	Extension flag	00	0	1	0：1個EDID；N-1：N个EDID
7F	Checksum	CD	205	-	Checksum

17.0 GENERAL PRECAUTIONS

17.1 HANDLING

(1) When the module is assembled, It should be attached to the system firmly using every mounting holes. Be careful not to twist or bend the modules.

(2) Refrain from strong mechanical shock or any force to the module. Otherwise, it may cause improper operation or damage to the module.

(3) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than 1 HB pencil lead.

(4) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use Ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth .In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static , it may cause damage to the module.

(9) Use fingerstalls with soft gloves to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Do not pull or fold the LED FPC.

(12) Do not touch any component which is located on the back side.

(13) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(14) Pins of connector shall not be touched directly with bare hands.

17.2 STORAGE

(1) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃ and relative humidity of less than 70%.

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.

17.3 OPERATION

(1) Do not connect, disconnect the module in the " Power On" condition.

(2) Power supply should always be turned on/off by following item 8.0 " Power on/off sequence ".

(3) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

(4) The standard limited warranty is only applicable when the module is used for general notebook applications. If used for purposes other than as specified, BOE is not to be held reliable for the defective operations. It is strongly recommended to contact BOE to find out fitness for a particular purpose.

17.4 OTHERS

(1) Avoid condensation of water. It may result in improper operation or disconnection of electrode.

(2) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation, Variation in part contents and environmental temperature, so on) Otherwise the module may be damaged.

(3) If the module displays the same pattern continuously for a long period of time, it can be the situation when The " image sticks" to the screen.

(4) This module has its circuitry PCB's on the rear or bottom side and should be handled carefully to avoid being stressed.

Appendix A

The Measurement Methods for the Dimensions of Module

1.Caliper:
Thickness of Outline (Without/With PCB)

2.Coordinate Measuring Machine:
a. Length of Outline (Without Tape Wrinkle or Bulged)
b. Width of Outline (Without PCB) (Without Tape Wrinkle or Bulged)
c. Width of Outline (With PCB)
d. CF Polarizer Size
e. Active Area (Or AA_BM) Size
f. Active Area to Outline (Without Tape Wrinkle or Bulged)
g. Active Area to CF Polarizer
h. The Distance of Bracket Holes
i. P-Cover to Outline (Without Tape Wrinkle or Bulged)
j. Length of P-Cover
k. Connector Pin 1 to Outline (Without Tape Wrinkle or Bulged)

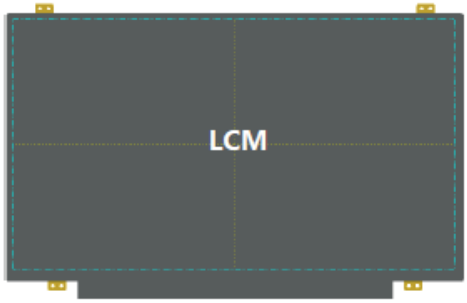
3. Height Gauge: The Different Height of Root and Top on the Bracket
(Need to Calculate From Bracket Angle Spec.)

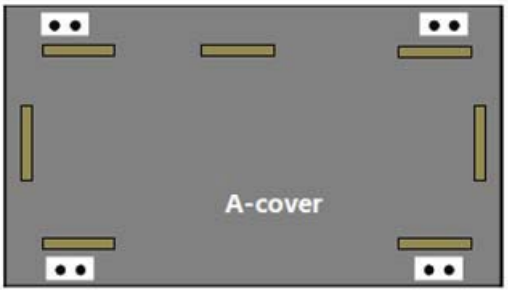
4.Feeler Gauge: The Warpage Spec. of Module

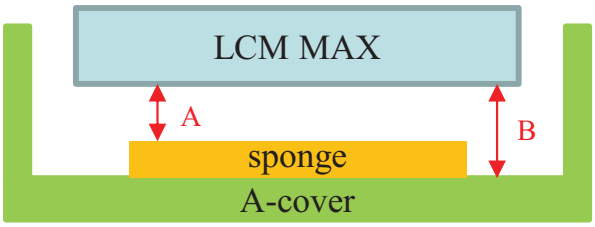
Notes:
Except the Critical Dimensions as Above, Other Dimensions are Measured by Coordinate Measuring Machine If Necessary.

Appendix B

LCM to A-Cover / sponges z-gap







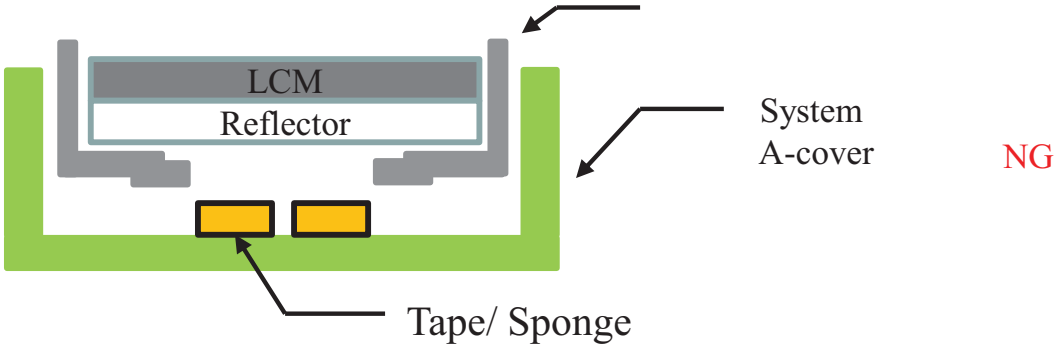
	Plastic Cover (LCM Thickness: Max)	Metal Cover (LCM Thickness: Max)
A	>0mm	>0mm
B	Min: 1.0mm	Min: 0.8mm
Without the open area of back cover		

Purpose	The reflector area is very sensitive, we suggest that design enough z-gap to decrease the risk of water ripple, white spot and other abnormal display

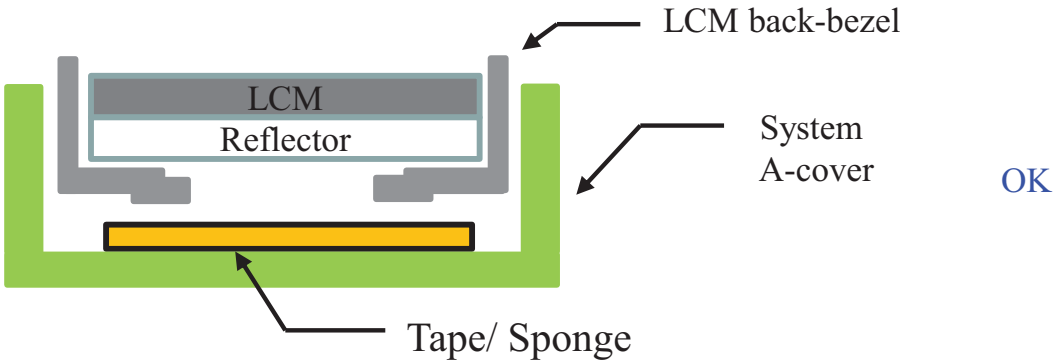
Appendix B

LCM to A-Cover / sponges z-gap

a



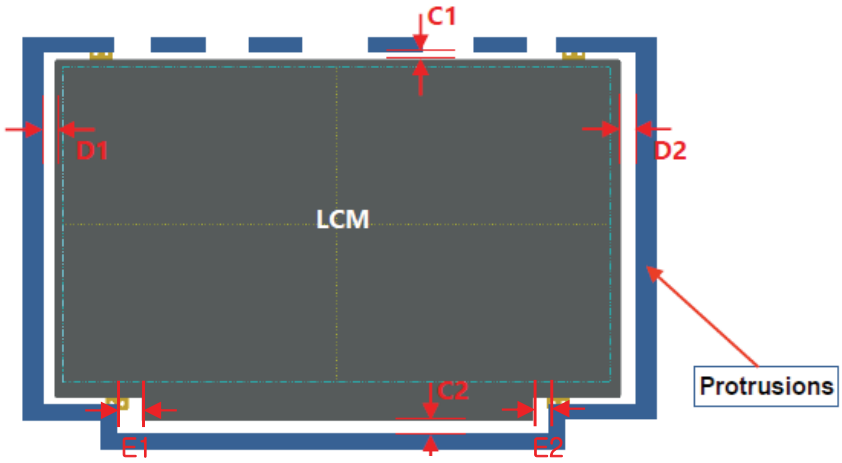
b



Purpose	If attach sponges or rubbers which correspond to white reflector area, it may cause white spot, pooling or other relate issues. We suggest that attach wide range sponges / rubbers which can cover the LCM back-bezel opening

Appendix B

LCM to side wall / protrusions



	Normal border	Narrow border
D1/D2	Min: 0.45mm	Min: 0.35mm
C1	Min: 0.50mm	
C2	Min: 0.50mm	
E1/E2	Min: 0.55mm	

Purpose	We suggest that design enough gap around LCM to prevent shock test failure, or interference, cell crack, abnormal display...etc. in the reliability test

Appendix B

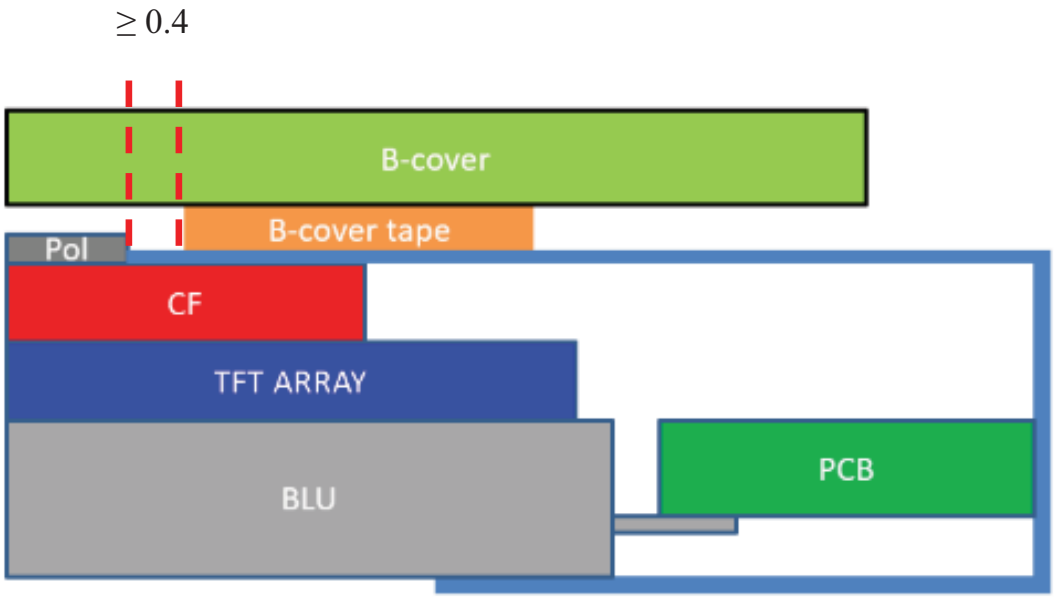
LCM to B-cover z-gap

B-cover Tape	Gap
Without	0.15 ~ 0.25mm
With	0.15 ~ 0.20mm

Purpose	Too less z-gap between system B-cover and LCM top pol has high risk to cause cell crack, pooling, light leakage and other issues

Appendix B

B-cover tape to top pol edge

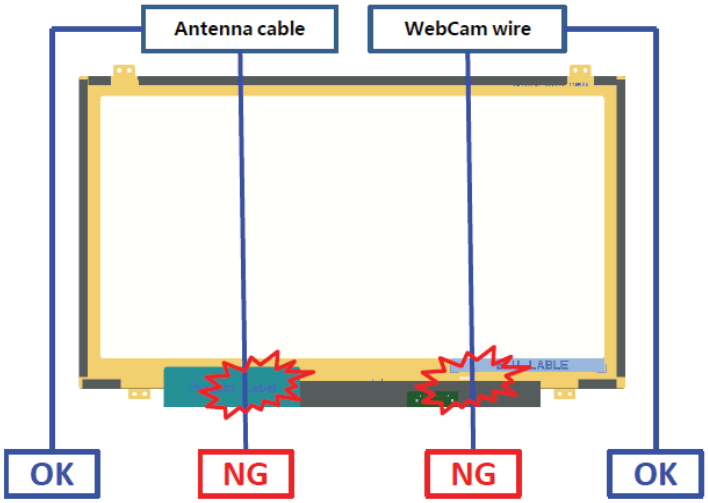


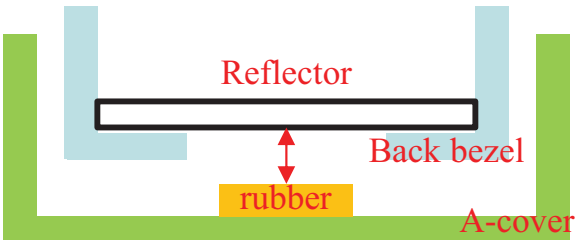
If attach b-cover and LCM with tapes,
Please let tapes to be located out of top pol edges 0.4mm away on 4 sides

Purpose	To avoid the B-cover tape override top pol and cause pooling or light leakage issue

Appendix B

Antenna Cable & Webcam wire



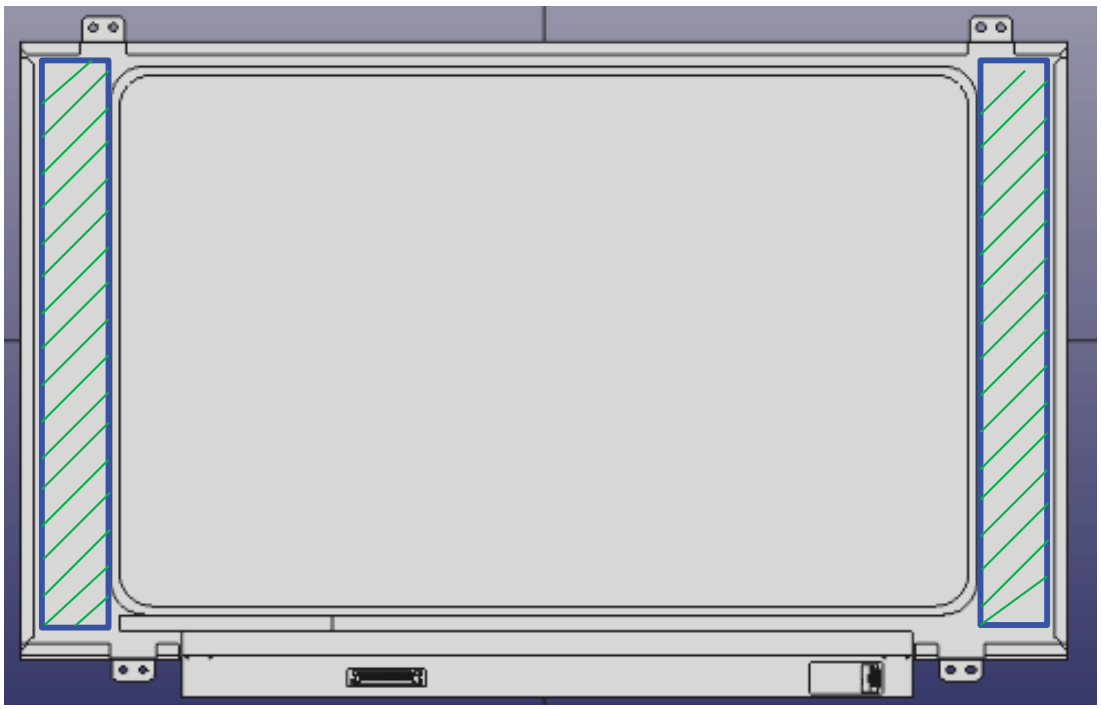


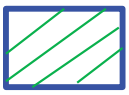
If sponge within the reflector area is necessary, we suggest that the gap between reflector and sponge is more than 0.5mm

Purpose	1. We suggest that do not set Antenna or WebCam cable / wire go behind LCM to avoid backpack test, hinge test ,twist test or pogo test with abnormal display 2. If the cable / wire is necessary to go behind LCM, please make a groove with rounds or chamfers to protect the cable / wire, or attach with higher sponge / rubbers adjacent to the cable / wire route 3. Suggest that attach the cable / wire with tapes to A-cover 4. Do not attach anything with LCM reflector area. If attach cable / wire with LCM reflector area, it may cause pooling, white spot, light leakage and other related issues

Appendix B

LCM paste area



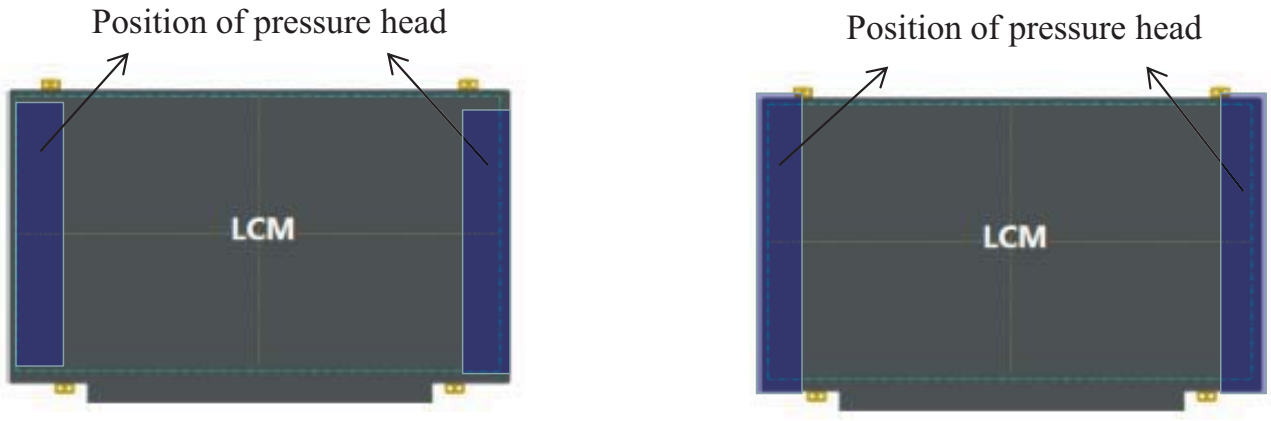


Attachment area

Purpose	If use the stretch remove tapes to fix LCM with A-cover, please set the stretch remove tapes correspond to the LCM back-bezel and do not let the tapes override the back-bezel's level step of opening

Appendix B

LCM pressable area

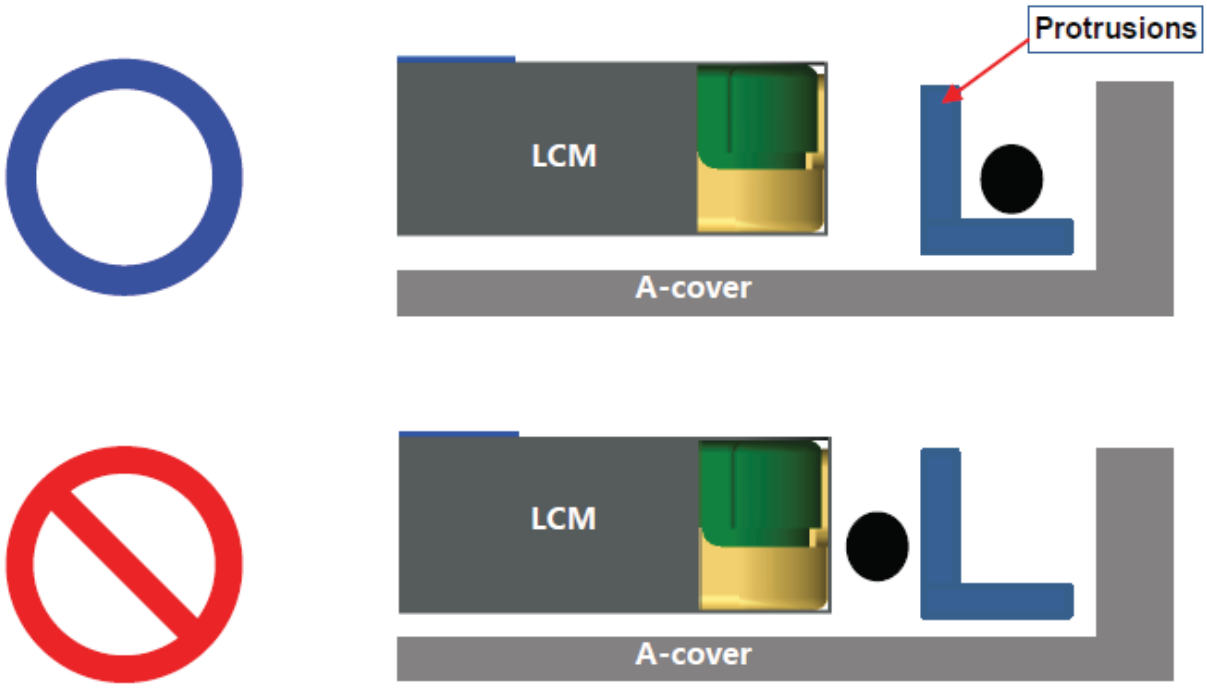


NG OK

Purpose	1. LCM is fixed on A-cover by double-sided tap which can stick LCM after using the press jig stress LCM during assembling. 2. To avoid panel broken the design of pressure head of press jig can not only pin on cell panel. The pressure head needs to pin on the LCM frame, which the LCM frame can share the pressure of the pressing head.

Appendix B

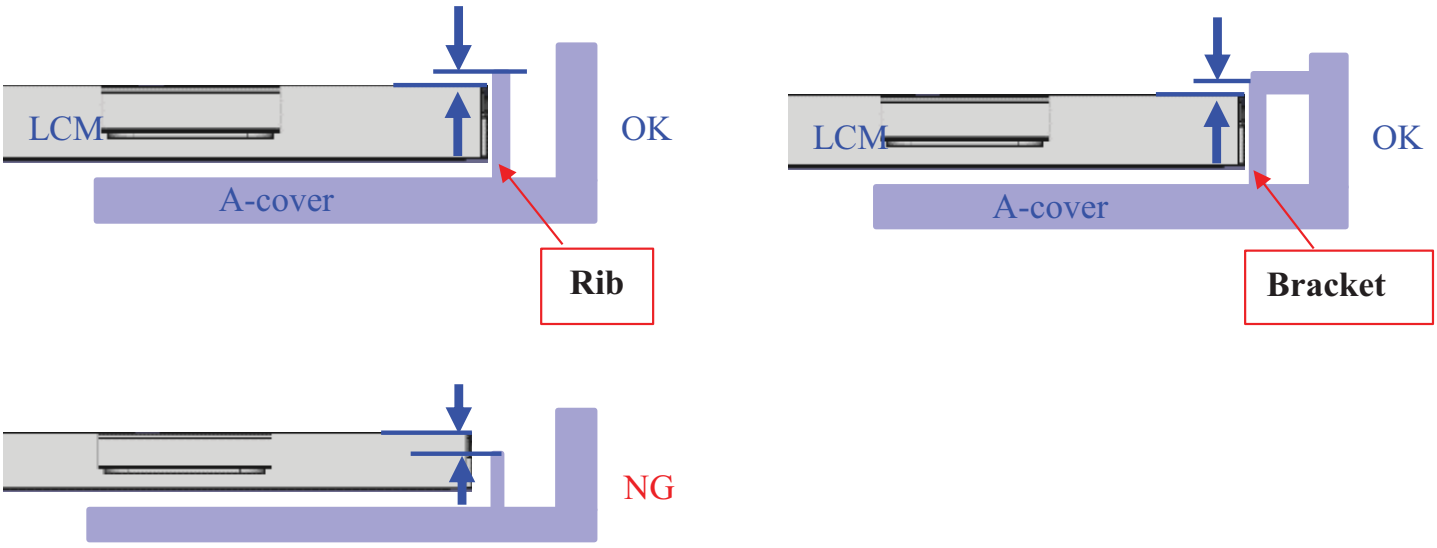
Wire setting



Purpose	Wire should be placed between Protrusions and A-cover. If place the wire between LCM and Protrusions, it may interfere with LCM when assembling B-covers, or even cause LCM breakage in reliability test.

Appendix B

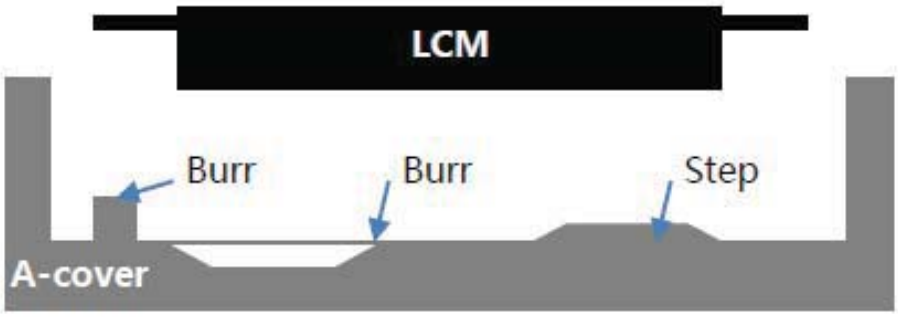
A-cover strength



Purpose	1. It is recommended that Rib height is higher than LCM, in order to avoiding press on LCM edge panels. 2. As for LCM is more stronger than Rib, the L Bracket is be recommended.

Appendix B

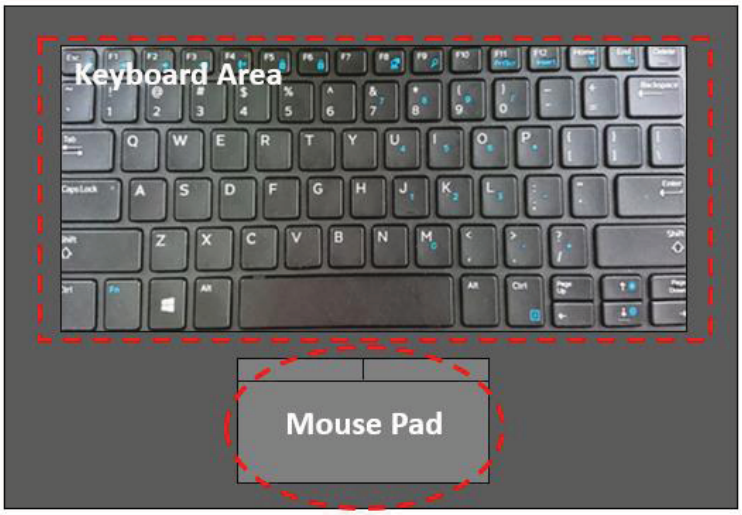
System A-cover Inner Surface

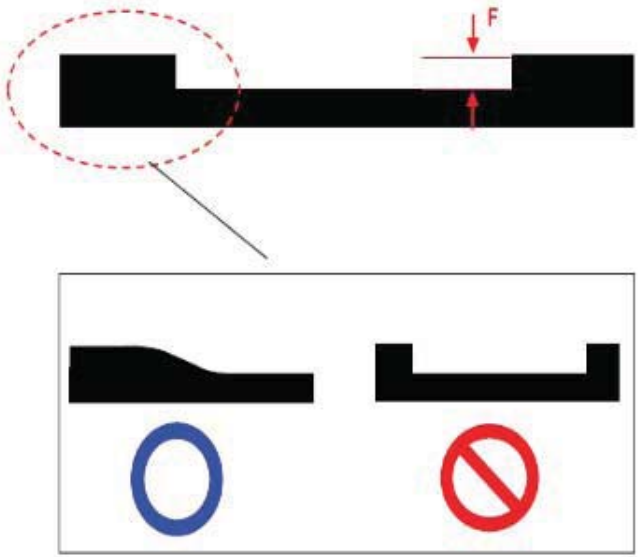


Purpose	There should not exist any burr, segment gap or protrusions beside Logo, which would cause White Spot or Glass Broken by stress concentration.

Appendix B

Keyboard area & Mouse pad



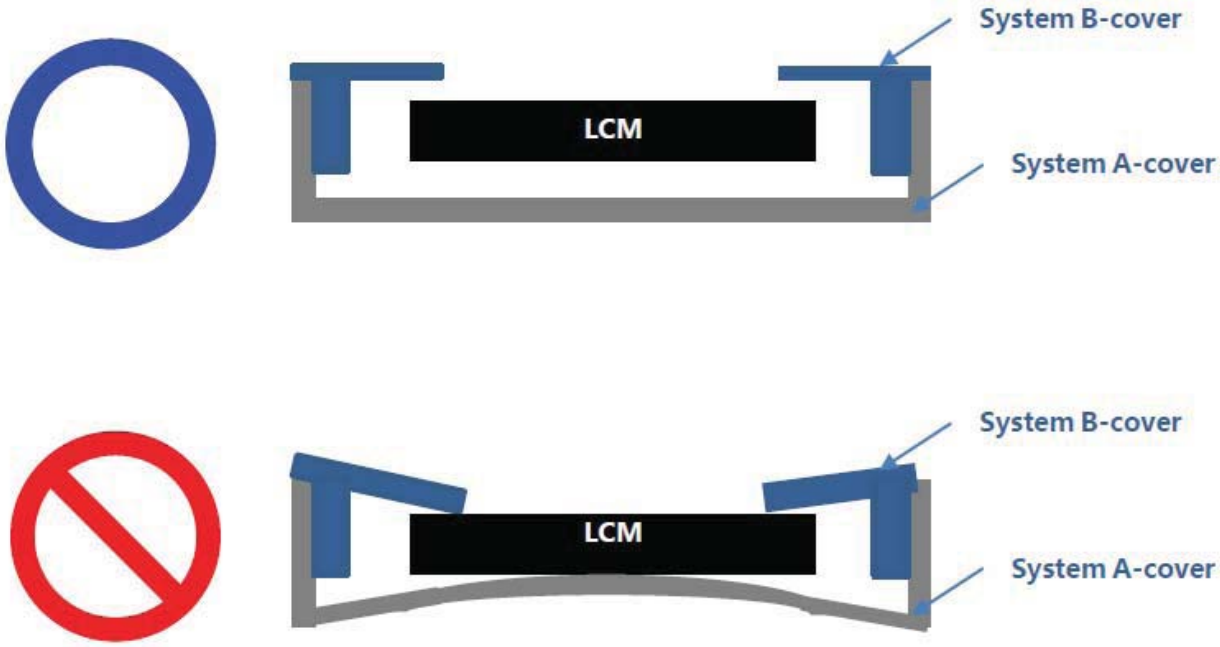


- F: max 0.3mm

Purpose	In order to avoiding LCM fragments in reliability test, the step surface of Keyboard and Mouse pad transmits smoothly, and should not be right-angle. For example, when Pogo testing, if the broken hole is done in this location, it is easy to produce fragments.

Appendix B

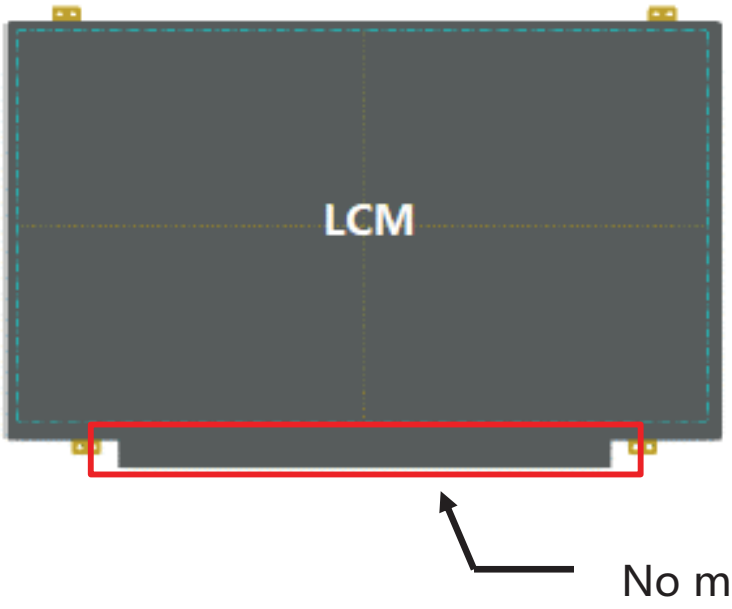
System cover reliability



Purpose	The permanent deformation part of System cover after the reliability test, including sponge and other structures or components, can not touch LCM.

Appendix B

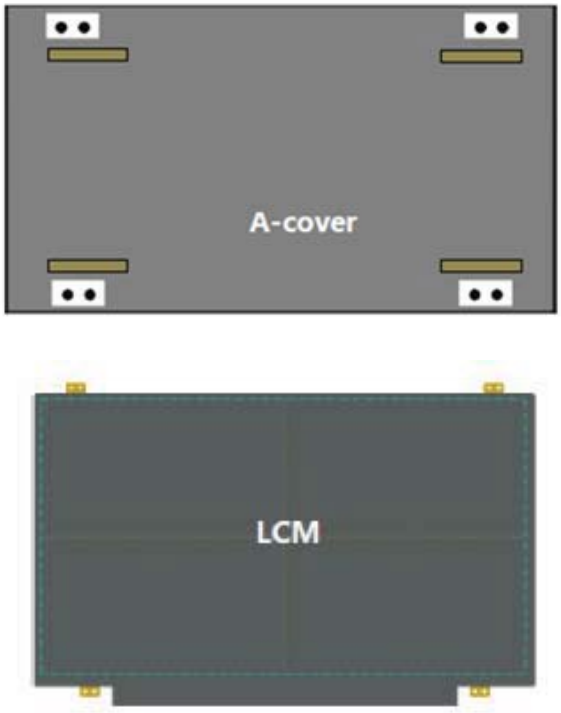
A/B-cover near LCD PCBA



Purpose	There should not have magnet object near LCM PCBA, which is prone to cause physical or electricity noise issue

Appendix B

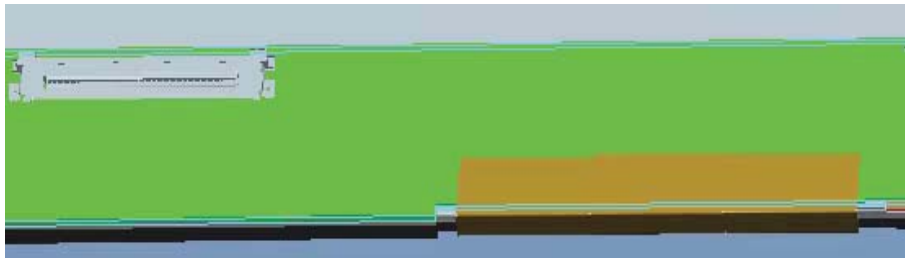
A-cover add sponges on Boss side wall

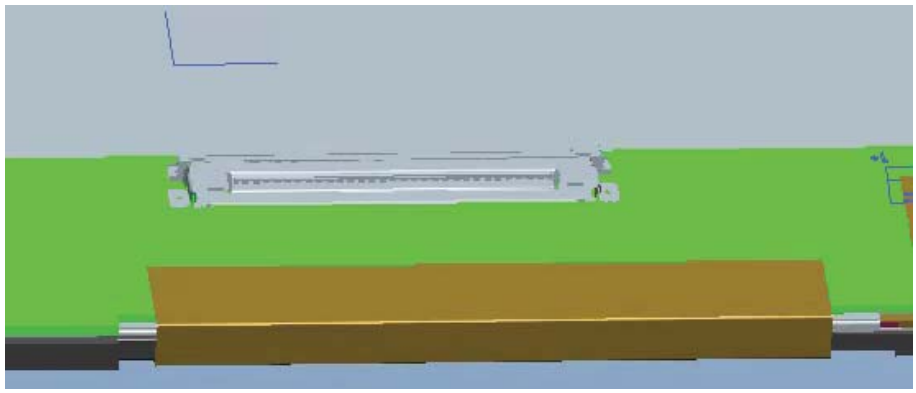


Purpose	We suggest to attach Sponges to the side of the Boss column of A-cover to reduce the panel broken possibility in assembly. It is recommended to this design synchronously.

Appendix B

LCM to A-Cover / sponges z-gap

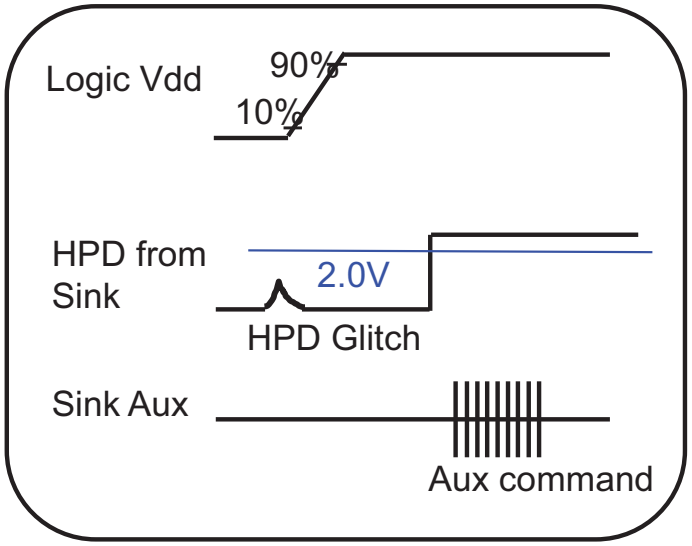




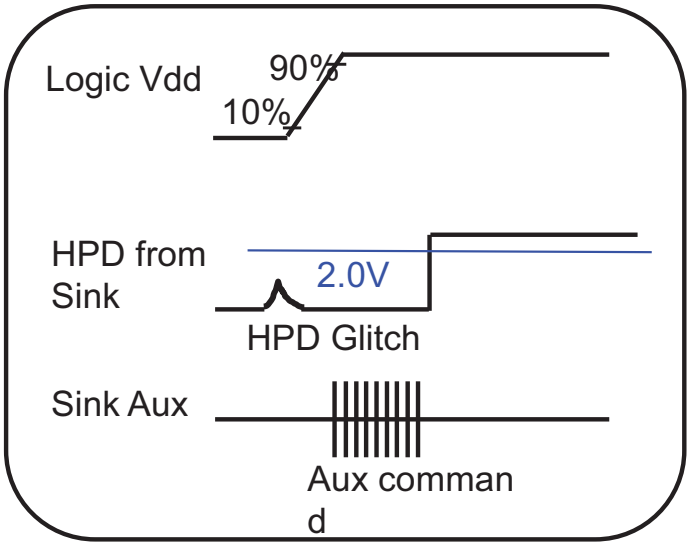
Purpose	Bent product: The position of system connector and FPC should be staggered in X direction. Otherwise, when testing, the system Cable line extrudes FPC, leading to FPC Crack; (Panel FPC Bonding location is related to Mask and can not be changed easily)

Appendix C

HPD Signal recognition



Normal Signal (Ignore HPD Glitch)

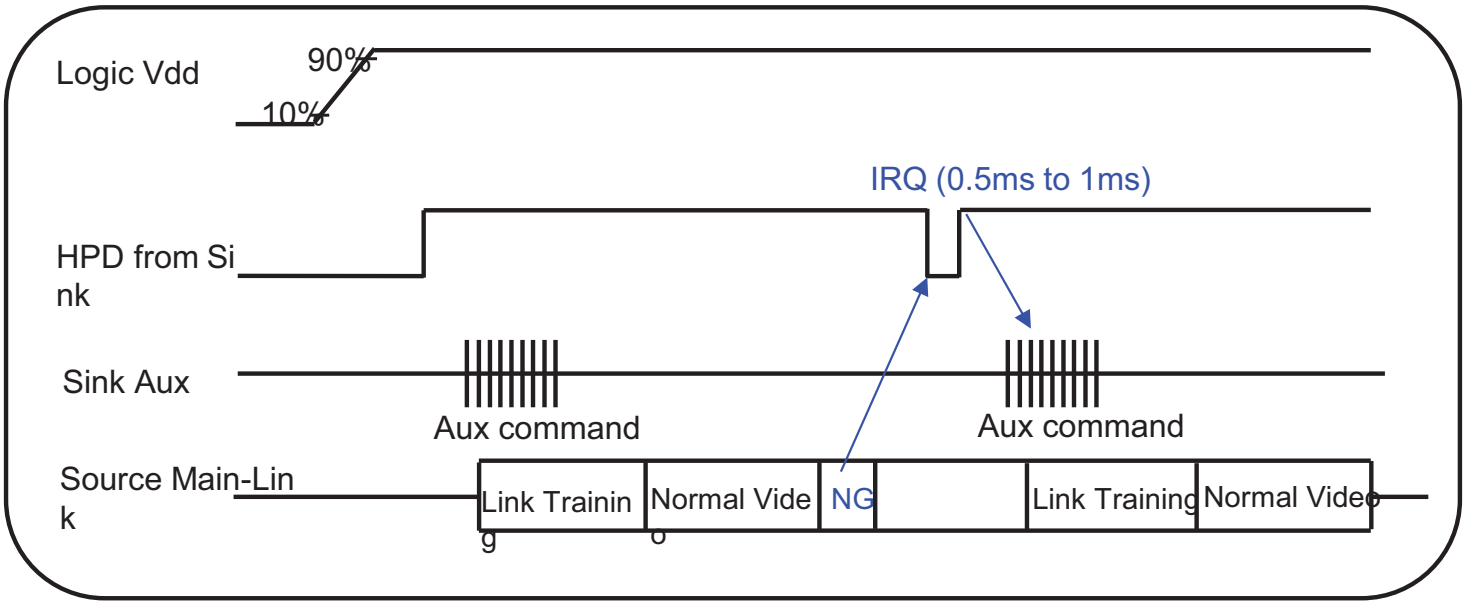


Abnormal Signal

Purpose	When HPD glitch of source device minimum is 2.0(V).

Appendix C

HPD Signal Definition IRQ (Interrupt Request)



Purpose	When HPD signal low than 0.5ms to 1ms, the source device should check sink status field from the DPCD and take link training again.

Appendix C

Main link eye diagram of TP3

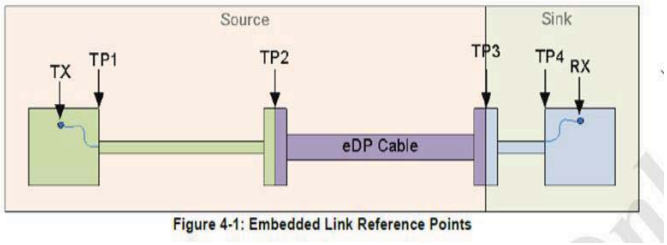
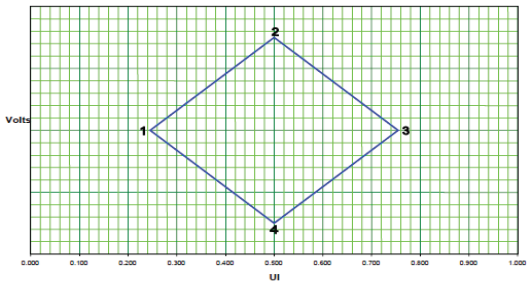


Figure 4-1: Embedded Link Reference Points

Measured TP3 on LCM connector.



Downstream Device Mask at TP3

	UI	Voltage
1	0.246	0
2	0.5	0.075
3	0.755	0
4	0.5	-0.075

Eye for TP3 at HBR

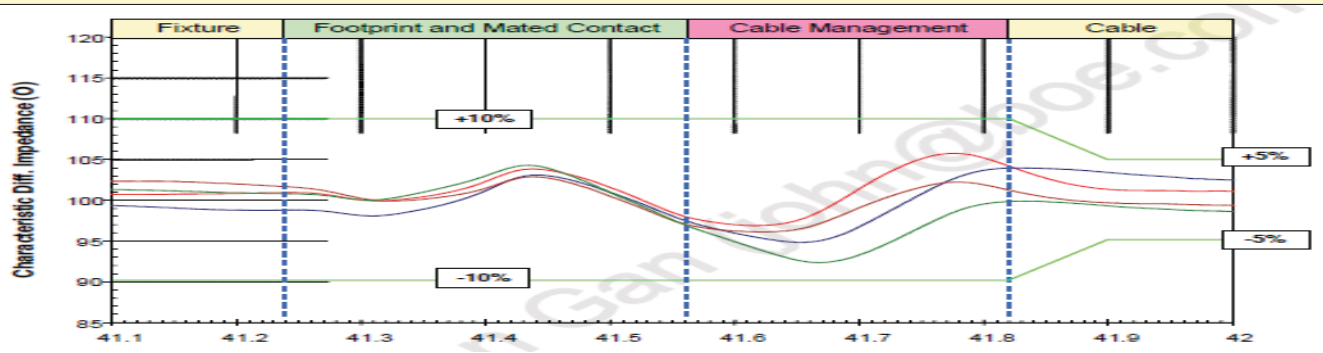
	UI	Voltage
1	0.375	0
2	0.5	0.023
3	0.625	0
4	0.5	-0.023

Eye for TP3 at RBR

Purpose	1. Main Link EYE Diagram should meet TP3 point of VESA. 2. The measure method is through access fixture.

Appendix C

Impedance Profile through a DP Connector



Differential Impedance Profile Measurement Data Example

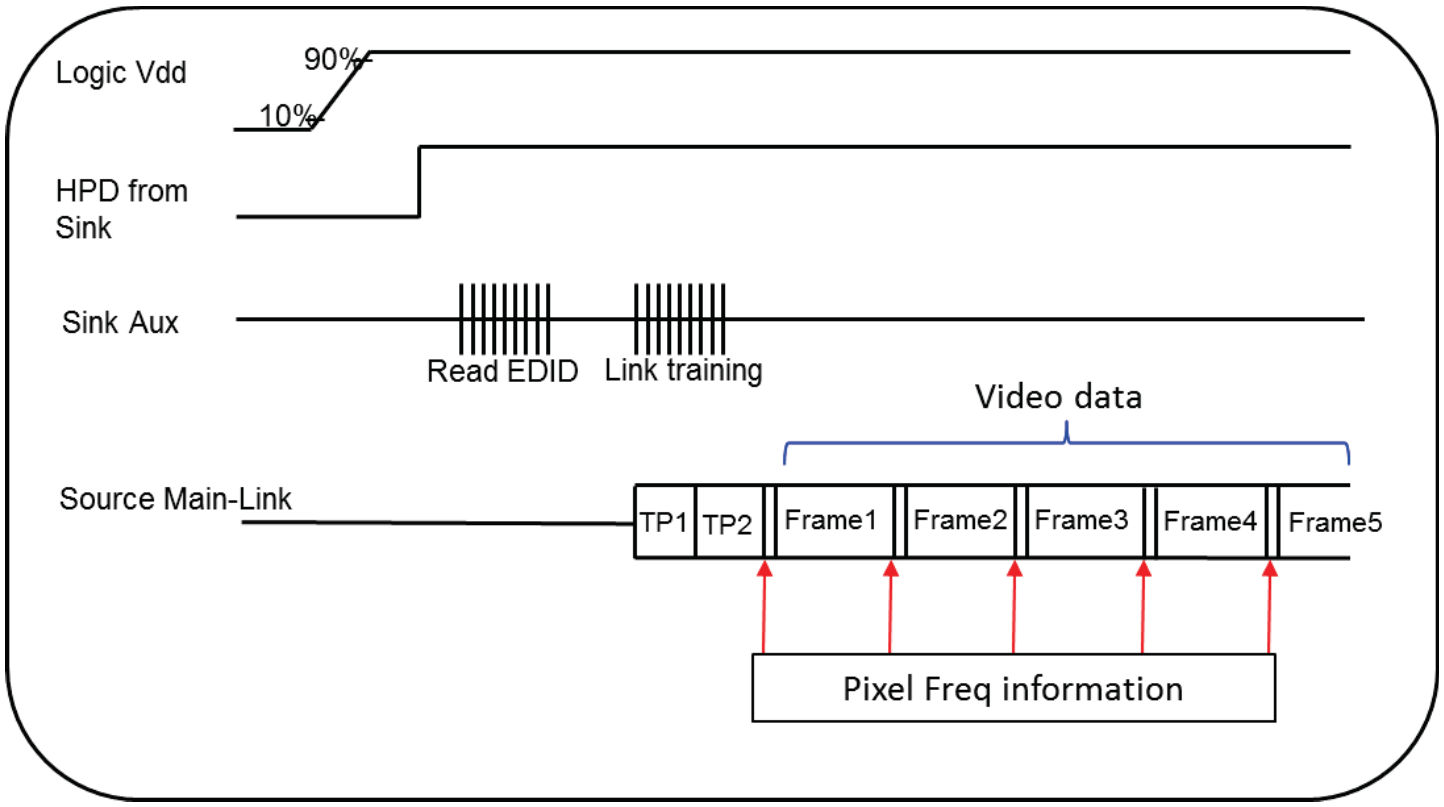
Segment	Differential Impedance Value	Maximum Tolerance
Fixture	100Ω/85Ω VESA	±10%
Connector	100Ω/85Ω VESA	±10%
Wire management	100Ω/85Ω VESA	±10%
Cable	100Ω/85Ω VESA	±5%

Impedance Profile Values for Cable Assembly

Purpose	Cable Impedance Profile 100ohm for Cable Assembly

Appendix C

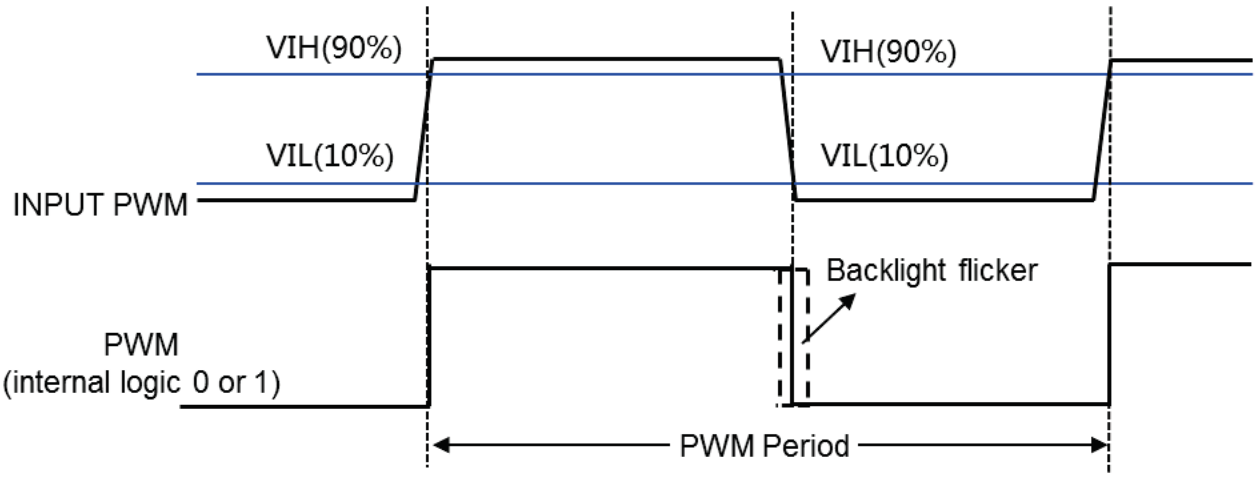
Main Link Pixel Freq information value of MSA data



Purpose	1. It need to fix pixel freq information value of MSA data output to prevent the initial abnormal pixel freq information value from incoming after power on. 2. BOE can read DPCD to check this value. Ex: BIOS is 1.62G , but into windows is 2.7G.

Appendix C

Main Link Pixel Freq information value of MSA data



Example:

Freq	Cycle Time	PWM Rising Time	PWM Falling Time
200Hz	5ms	≤1us	≤1us
1KHz	1ms	≤200ns	≤200ns

Purpose	1. LED driver need to calculate the duty cycle of input PWM signal. 2. To avoid backlight flicker visible on LCD, system input PWM suggest : PWM rising ≤ 200ppm*cycle time ; PWM falling ≤ 200ppm*cycle time.